

| PAGE | TITLE |
|------|-----------------------------|
| 01 | INDEX |
| 02 | BLOCK DIAGRAM |
| 03 | CLOCKS DIAGRAM |
| 04 | POWER DISTRIBUTION |
| 05 | POWER FLOW |
| 06 | STRAP & GPIO |
| 07 | POWER SEQUENCE DIAGRAM |
| 08 | INTERRUPT & PME DIAGRAM |
| 09 | CPU XDP |
| 10 | MCP- CLK/CTRL/MISC/DEBUG |
| 11 | MCP- DDR4 CHANNEL A & B |
| 12 | MCP- PCI/DMI/DDI |
| 13 | MCP- POWER CONNECTIONS |
| 14 | MCP- VSS |
| 15 | BLANK |
| 16 | DDR4 CHA XIMM1 |
| 17 | DDR4 CHB XIMM2 |
| 18 | GFX M.2 SLOT |
| 19 | BLANK |
| 20 | PCH - DMI/PCIE/USB2-3 |
| 21 | PCH - SMBUS/HDA/GPIO/JTAG |
| 22 | PCH - SATA/SPI/GPIO |
| 23 | PCH - GPIO/MISC |
| 24 | PCH - CLOCK |
| 25 | PCH - PWR/STRAP |
| 26 | PCH-PLL FILTER & DECOUPLING |
| 27 | SPI ROM |
| 28 | TPM 9670 |
| 29 | BLANK |
| 30 | LAN_RTL8161GSH |
| 31 | CR_RTS5145 |
| 32 | AUDIO_CODEC_ALC3252 |
| 33 | AUDIO_CONNECTOR |
| 34 | BLANK |
| 35 | SIO ITE8656 |
| 36 | FAN |
| 37 | POWER_BTN |
| 38 | BLANK |
| 39 | USB 3.0 PWR |
| 40 | USB 3.0 CONN |
| 41 | USB 2.0 DONGLE |
| 42 | CC LOGIC |
| 43 | USB3 TYPE-C |
| 44 | FIO CONN |
| 45 | SATA CONN |
| 46 | M2_2280_SSD |
| 47 | M2_2230_WLAN |
| 48 | DP PORT |
| 49 | HDMI PORT |
| 50 | BLANK |
| 51 | LEDs/HOODLOCK_SENSE |
| 52 | HEADER/MECHANICAL PARTS |
| 53 | BLANK |
| 54 | POWER SEQUENCE |
| 55 | ADAPTER IN |
| 56 | +VCORE +VCCGT CONTROLLER |
| 57 | +VCORE PHASE 1 & 2 |
| 58 | +VCORE PHASE 3 |
| 59 | +VCCGT Phase 1 & 2 |
| 60 | +VCCIO |
| 61 | +VCCSA |
| 62 | +3V3_S5 & +5V_S5 |
| 63 | +1V_PCH |
| 64 | +12V |
| 65 | +VDDQ |
| 66 | +2V5_VPP |
| 67 | +5V & +3V3 |
| 68 | +VTT_DDR |
| 69 | +1V2 |
| 70 | CHANGE LIST |

Intel Sky Lake Plat f or m

SLK-S CPU(TDP 35W) / SLK PCH-H (H170)

Project Informat i on
Phase: SMVB
Ver: X9
SVID: 103C
SSID: 81C9
Form factor: mini DT


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| Marking | Description |
|---------|--------------------------|
| I | Installed |
| NI | Not Installed |
| MP | Production Part ONLY |
| PROTO | Not For Production Part |
| CCL | Critical Components List |

| PCB AND SILKSCREEN COLOR | | |
|--------------------------|--------------|------------|
| Program Phase | Color of PCB | Silkscreen |
| EVT | RED | YELLOW |
| DVT | LIGHT BLUE | YELLOW |
| PVT/MVB / PRODUCTION | GREEN | WHITE |

| | |
|----------------|-----|
| PCA P/N, TESLA | TBD |
| SCH P/N, TESLA | TBD |
| PCB P/N, TESLA | TBD |

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Size Document Number
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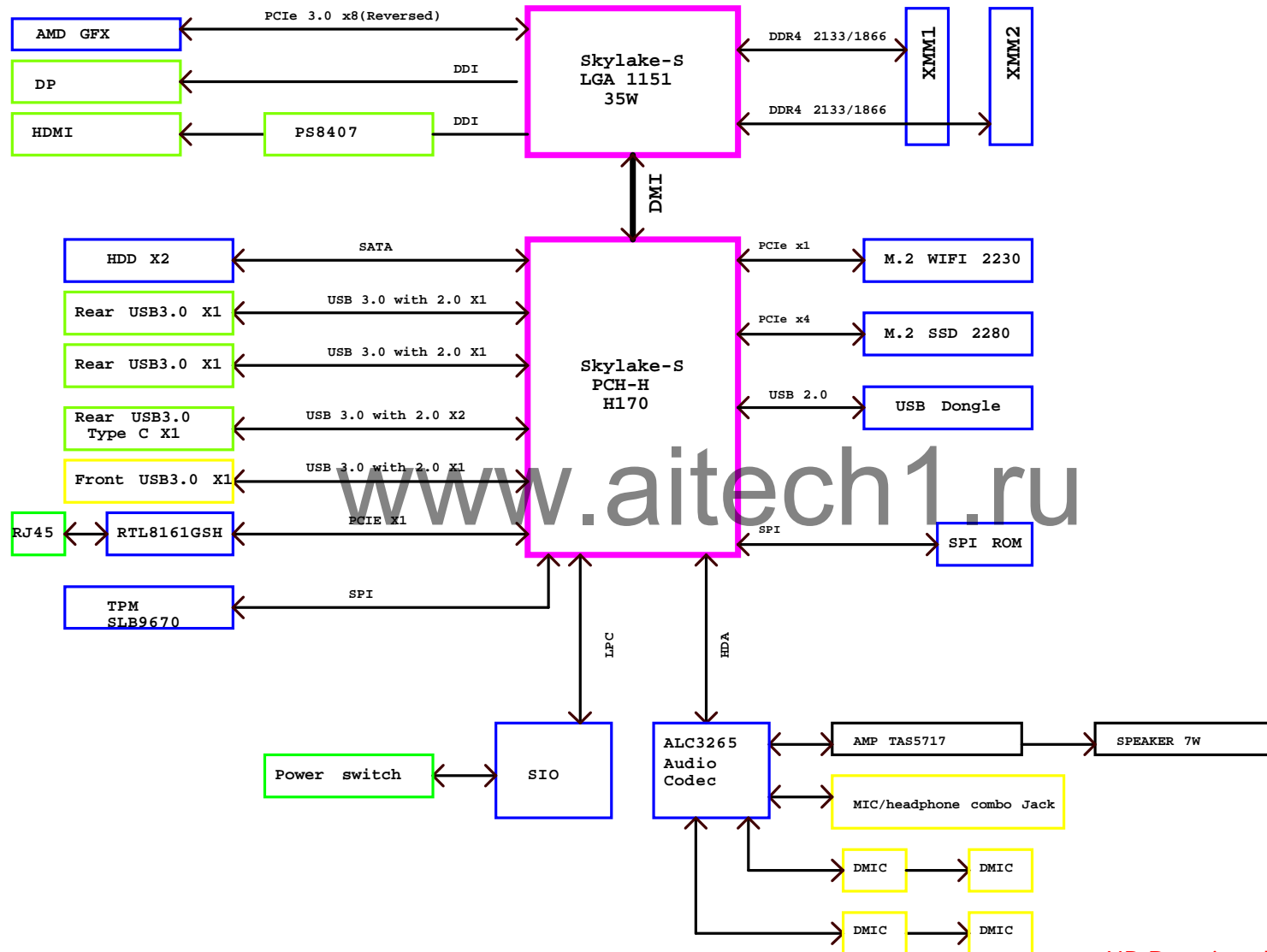
Sheet 1 of 70

Rev
X9


Front IO

Rear IO

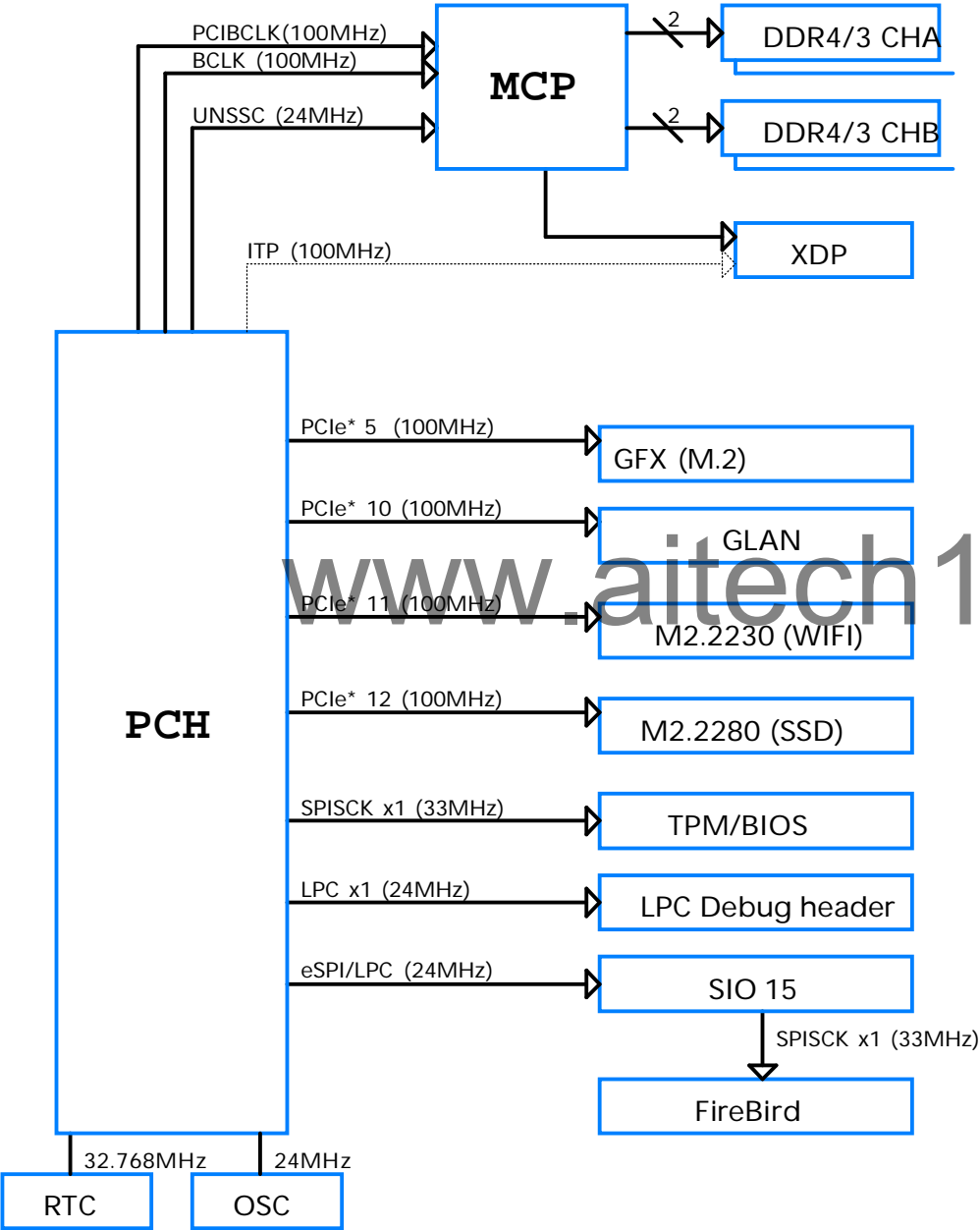
System BLOCK Diagram




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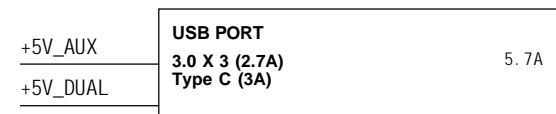
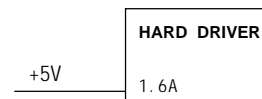
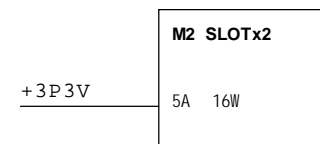
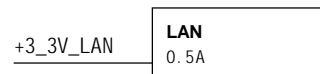
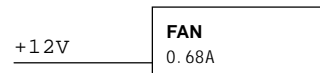
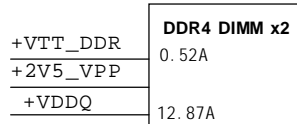
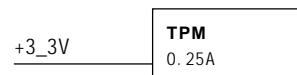
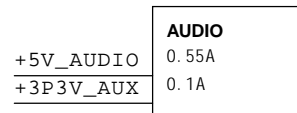
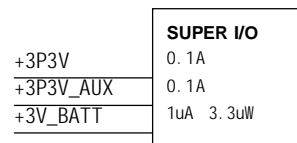
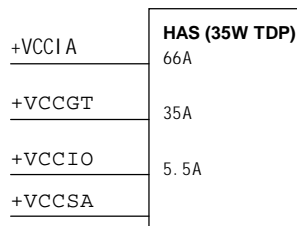
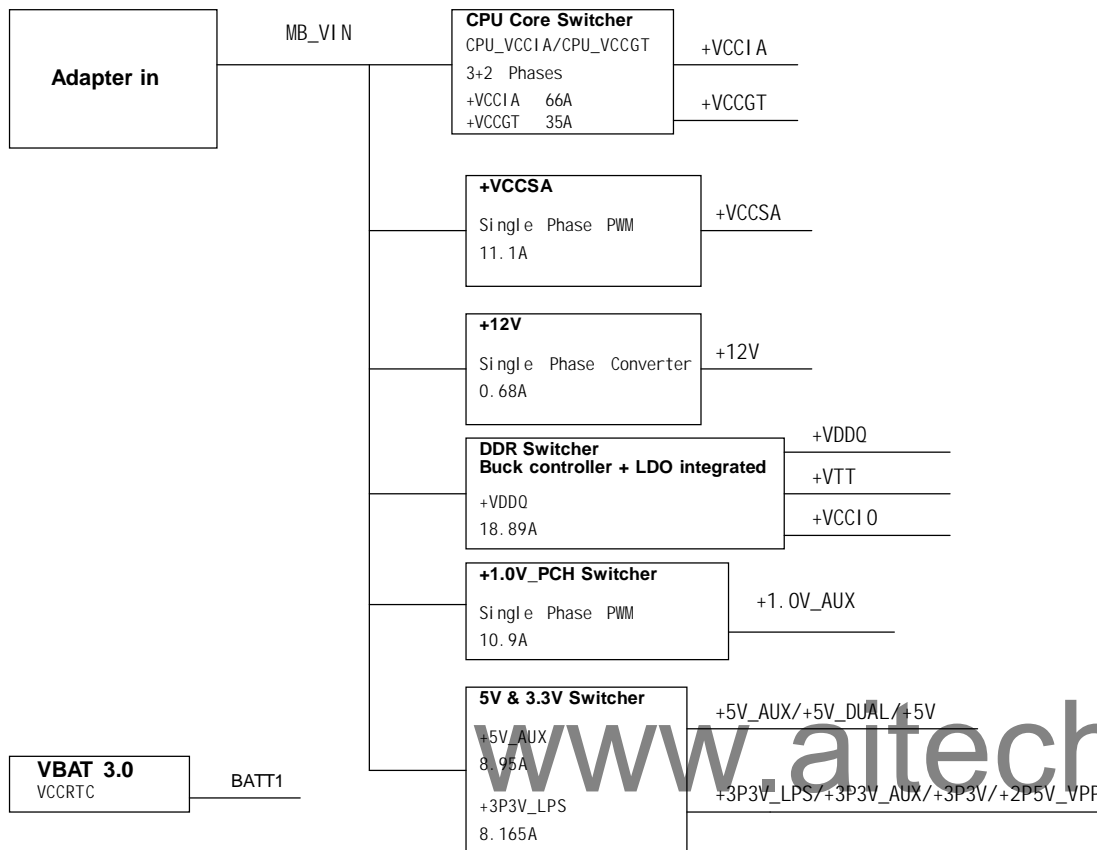
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Clock Diagram




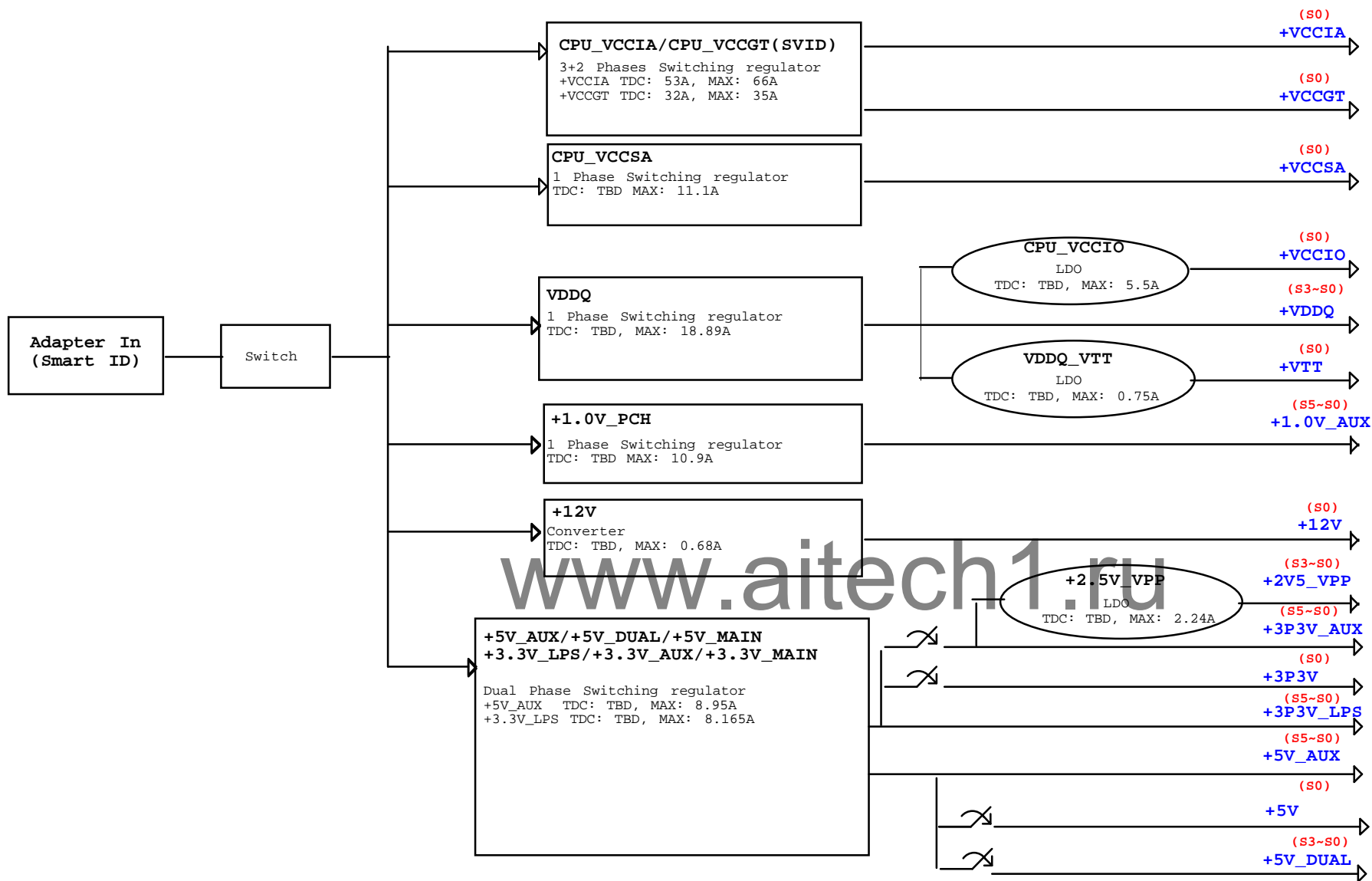
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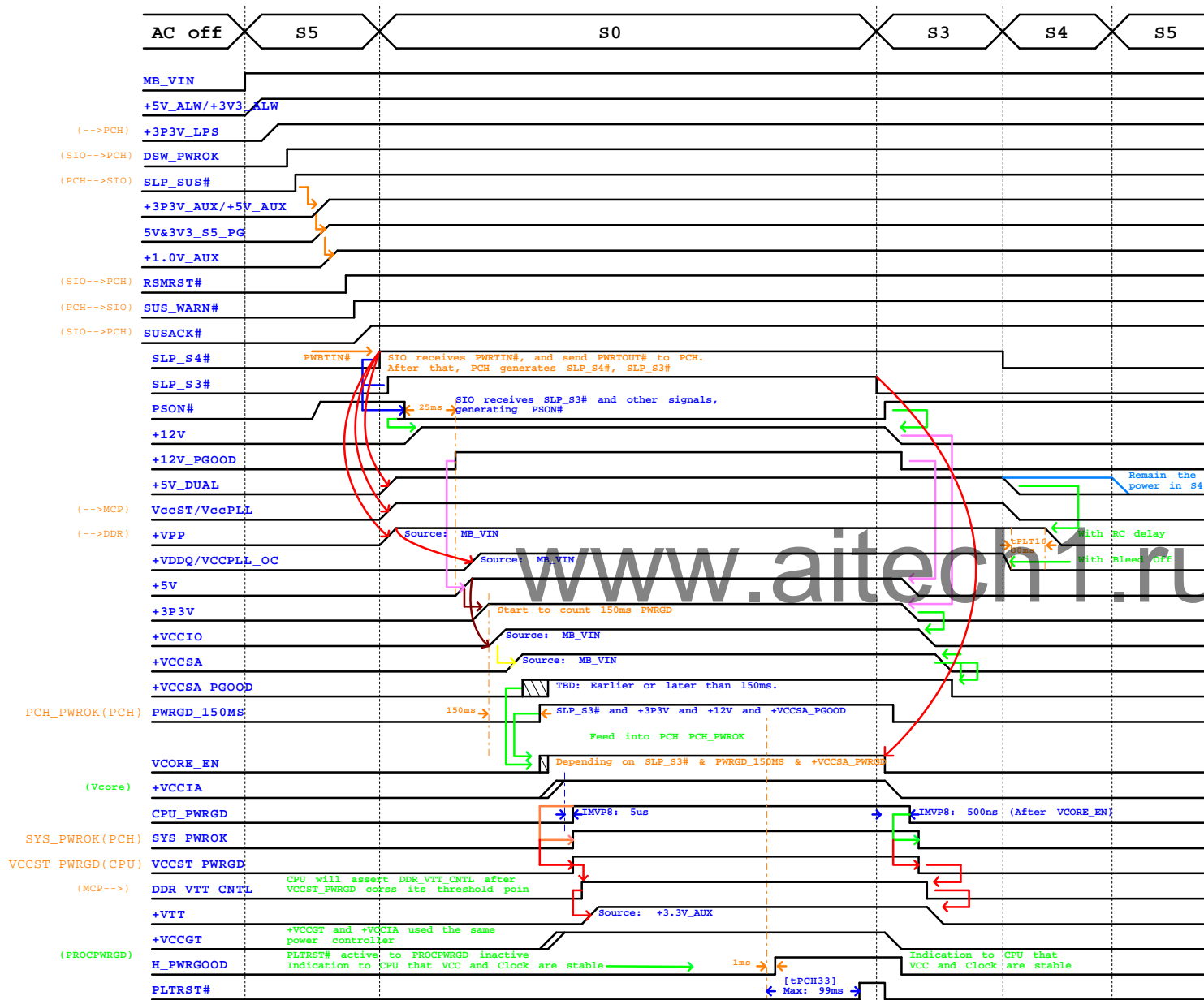
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| | | | | | X9 |
| Date: Monday, June 13, 2016 | | Sheet | | 5 | of 70 |

| Index | PCR Tests | Power Tests | Round Tests | Default Values | Internal MD Hashes | NOTE | Usage | Public Key | Group | Version | Power Tests |
|-------------------|---|----------------|----------------|----------------|--------------------|------|-------|------------|-------|---------|-------------|
| Group 0 (SHA-256) | SHA256_HASH_0 = SHA256(SHA256_HASH_0) | | | | | | | | | | |
| | GROUP_0 | SHA256_HASH_0 | SHA256_HASH_0 | GR0 | SHA256_HASH_0 | | None | None | None | None | |
| | GROUP_1 | SHA256_HASH_1 | SHA256_HASH_1 | GR1 | None | | None | None | None | None | |
| | GROUP_2 | SHA256_HASH_2 | SHA256_HASH_2 | GR2 | None | | None | None | None | None | |
| | GROUP_3 | SHA256_HASH_3 | SHA256_HASH_3 | GR3 | None | | None | None | None | None | |
| | GROUP_4 | SHA256_HASH_4 | SHA256_HASH_4 | GR4 | None | | None | None | None | None | |
| | GROUP_5 | SHA256_HASH_5 | SHA256_HASH_5 | GR5 | None | | None | None | None | None | |
| | GROUP_6 | SHA256_HASH_6 | SHA256_HASH_6 | GR6 | None | | None | None | None | None | |
| | GROUP_7 | SHA256_HASH_7 | SHA256_HASH_7 | GR7 | None | | None | None | None | None | |
| | GROUP_8 | SHA256_HASH_8 | SHA256_HASH_8 | GR8 | None | | None | None | None | None | |
| | GROUP_9 | SHA256_HASH_9 | SHA256_HASH_9 | GR9 | None | | None | None | None | None | |
| | GROUP_10 | SHA256_HASH_10 | SHA256_HASH_10 | GR10 | None | | None | None | None | None | |
| | GROUP_11 | SHA256_HASH_11 | SHA256_HASH_11 | GR11 | None | | None | None | None | None | |
| | GROUP_12 | SHA256_HASH_12 | SHA256_HASH_12 | GR12 | None | | None | None | None | None | |
| | GROUP_13 | SHA256_HASH_13 | SHA256_HASH_13 | GR13 | None | | None | None | None | None | |
| Group 1 (SHA-256) | SHA256_HASH_14 = SHA256(SHA256_HASH_14) | | | | | | | | | | |
| | GROUP_14 | SHA256_HASH_14 | SHA256_HASH_14 | GR14 | None | | None | None | None | None | |
| | GROUP_15 | SHA256_HASH_15 | SHA256_HASH_15 | GR15 | None | | None | None | None | None | |
| | GROUP_16 | SHA256_HASH_16 | SHA256_HASH_16 | GR16 | None | | None | None | None | None | |
| | GROUP_17 | SHA256_HASH_17 | SHA256_HASH_17 | GR17 | None | | None | None | None | None | |
| | GROUP_18 | SHA256_HASH_18 | SHA256_HASH_18 | GR18 | None | | None | None | None | None | |
| | GROUP_19 | SHA256_HASH_19 | SHA256_HASH_19 | GR19 | None | | None | None | None | None | |
| | GROUP_20 | SHA256_HASH_20 | SHA256_HASH_20 | GR20 | None | | None | None | None | None | |
| | GROUP_21 | SHA256_HASH_21 | SHA256_HASH_21 | GR21 | None | | None | None | None | None | |
| | GROUP_22 | SHA256_HASH_22 | SHA256_HASH_22 | GR22 | None | | None | None | None | None | |
| | GROUP_23 | SHA256_HASH_23 | SHA256_HASH_23 | GR23 | None | | None | None | None | None | |
| | GROUP_24 | SHA256_HASH_24 | SHA256_HASH_24 | GR24 | None | | None | None | None | None | |
| | GROUP_25 | SHA256_HASH_25 | SHA256_HASH_25 | GR25 | None | | None | None | None | None | |
| | GROUP_26 | SHA256_HASH_26 | SHA256_HASH_26 | GR26 | None | | None | None | None | None | |
| | GROUP_27 | SHA256_HASH_27 | SHA256_HASH_27 | GR27 | None | | None | None | None | None | |

[illegible][illegible]

POWER SEQUENCE DIAGRAM

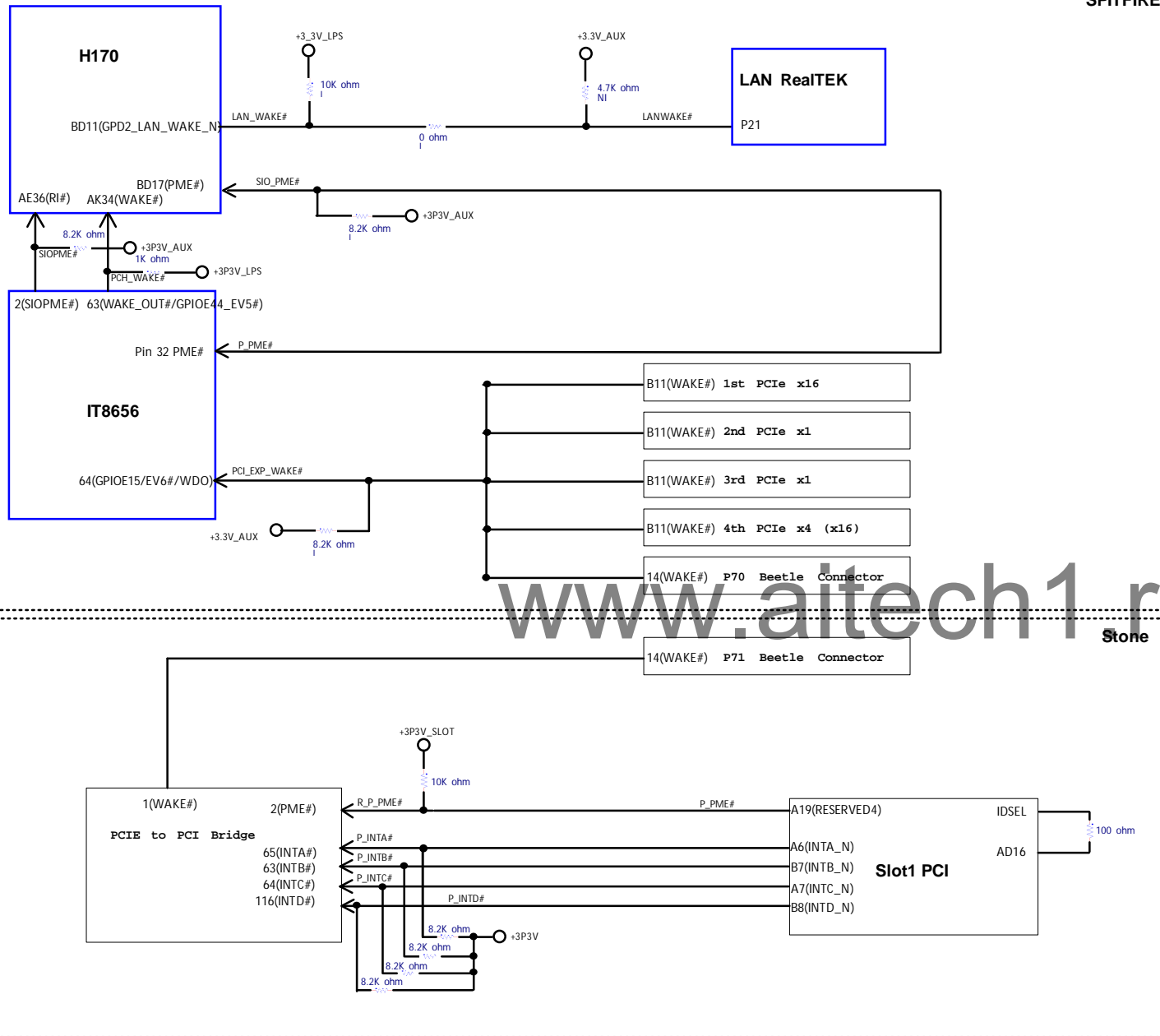


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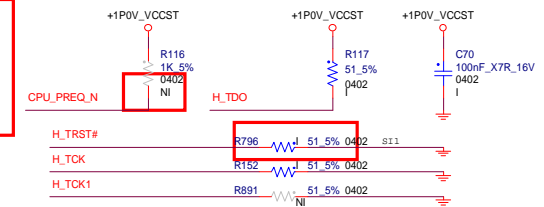
Interrupt & PME diagram

SPITFIRE

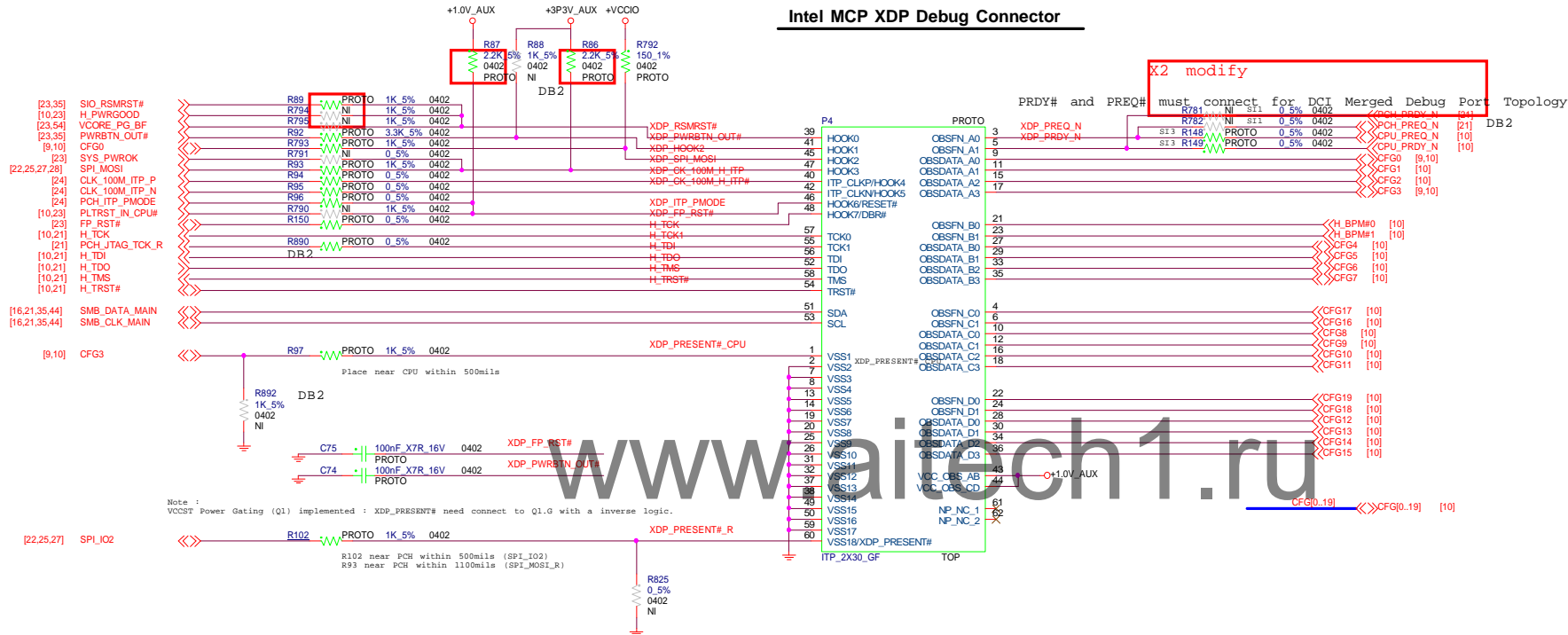


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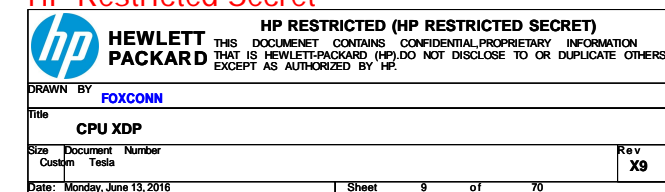
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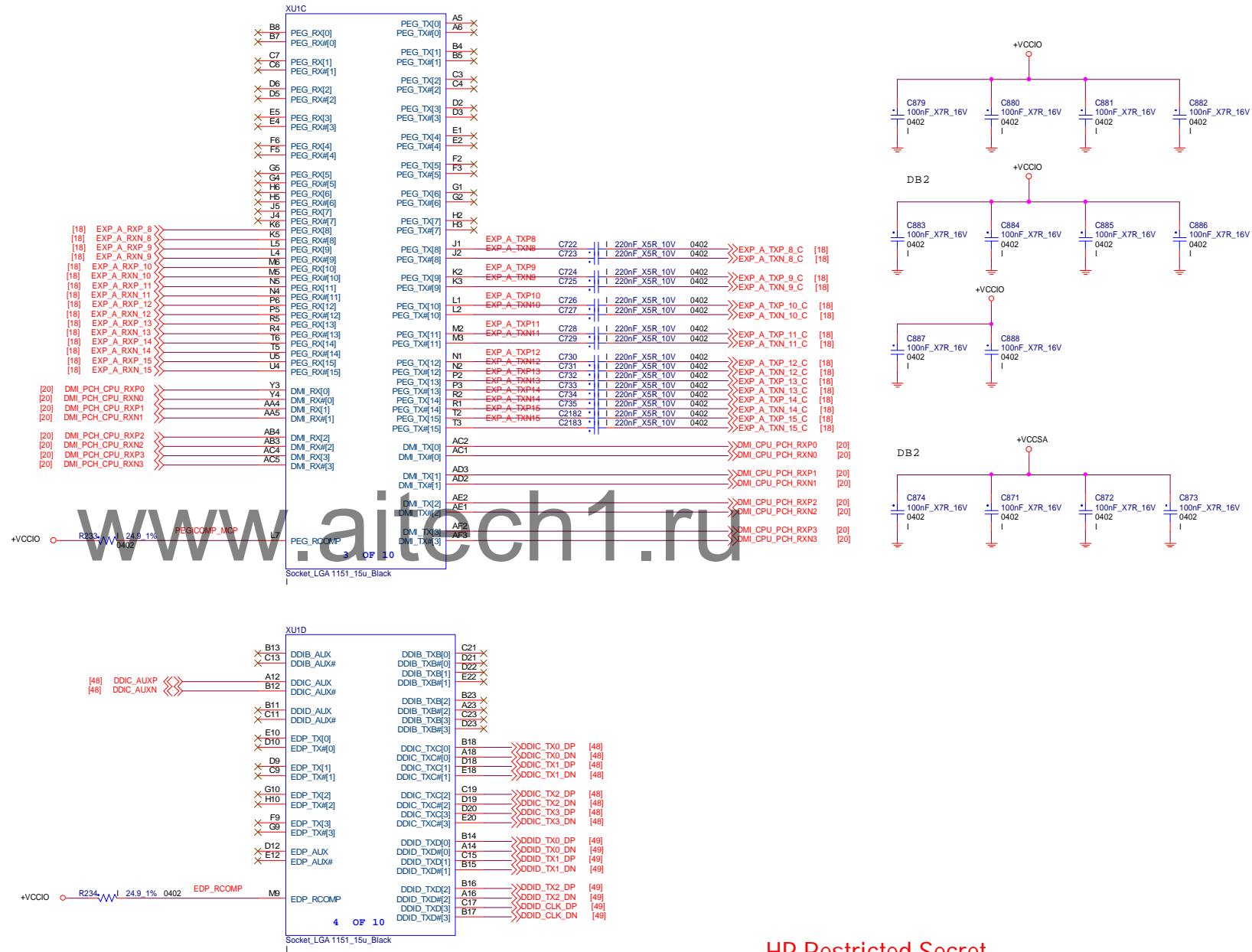
```
X2 modify
Q# must connect for DCI Merged Debug Por
R781 N SI1 0 5% 0402 42011 PPPX N 041
```



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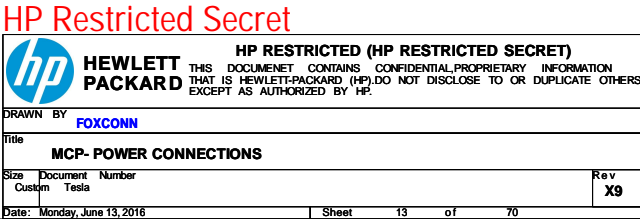


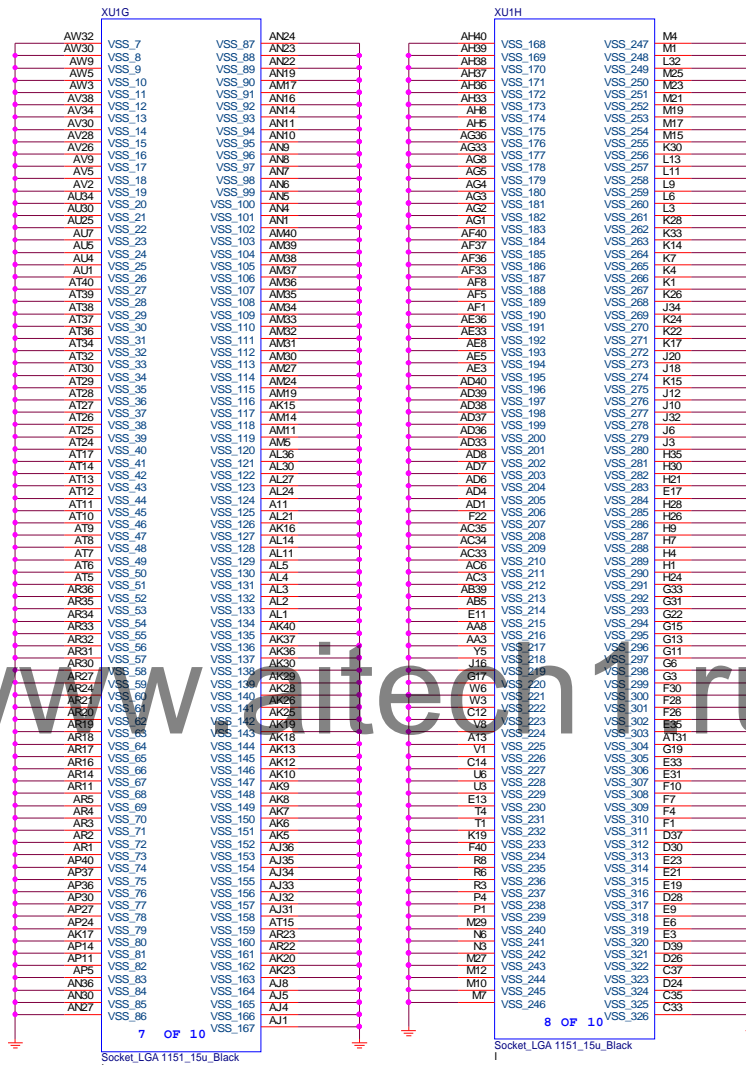
MCP - PCIE,DMI,FDI,DDI



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| Custom | Tesla | | X9 |
| Date: Monday, June 13, 2016 | | Sheet | 12 of 70 |





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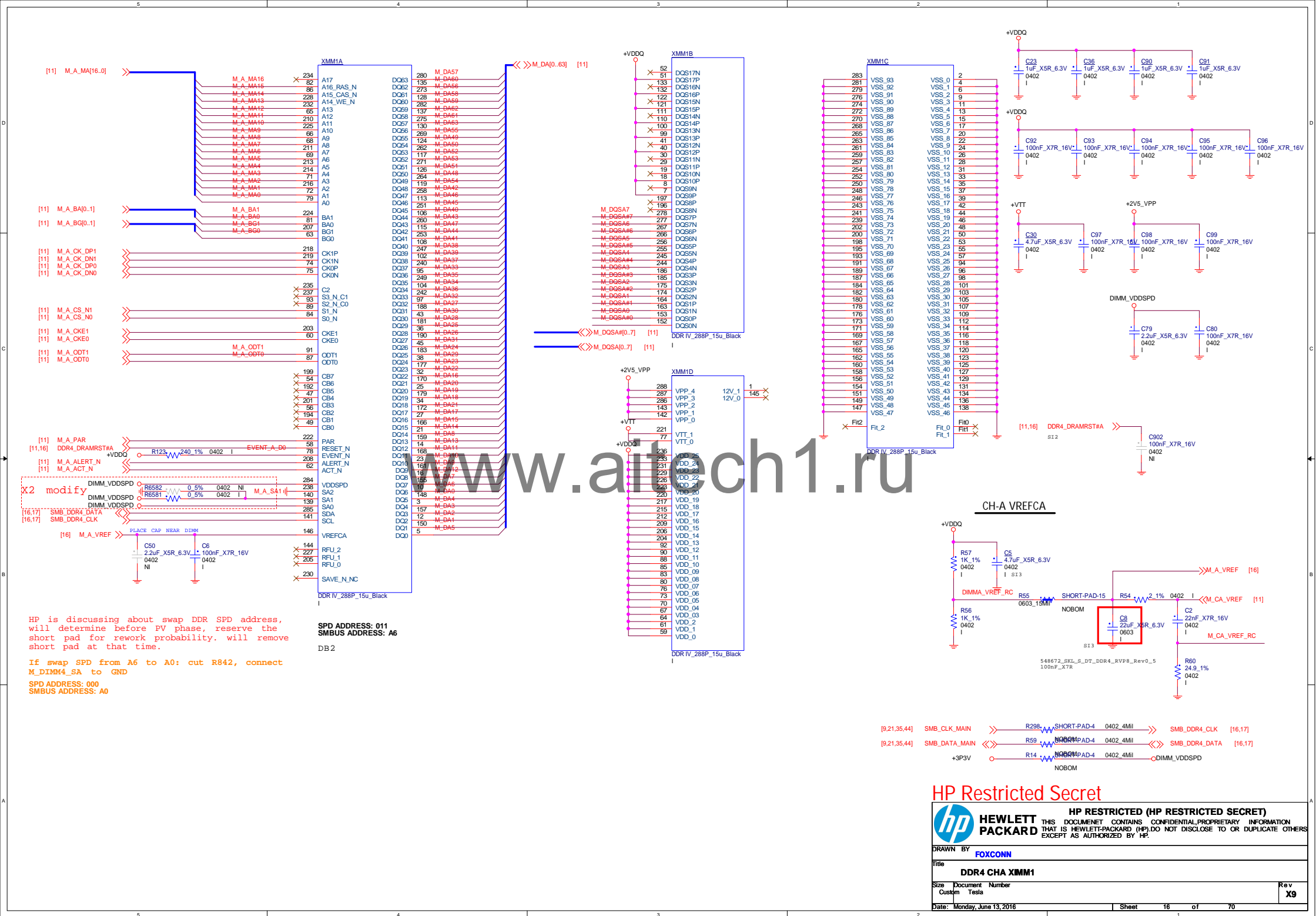
HP is discussing about swap DDR SPD address, will determine before PV phase, reserve the short pad for rework probability. will remove short pad at that time.

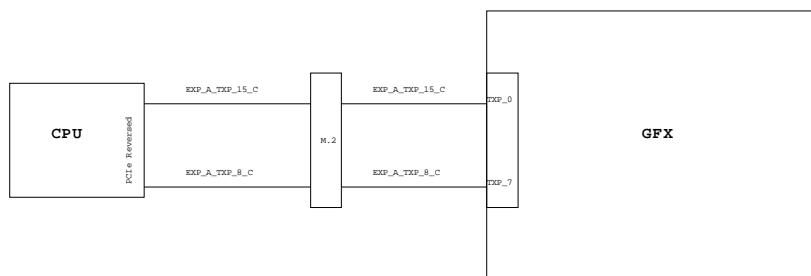
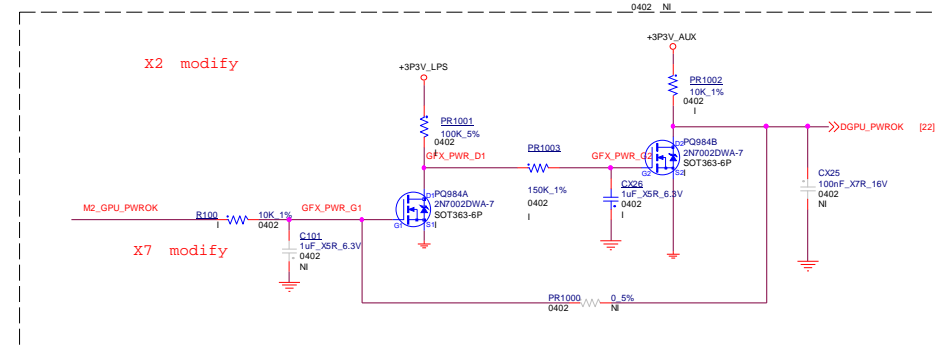
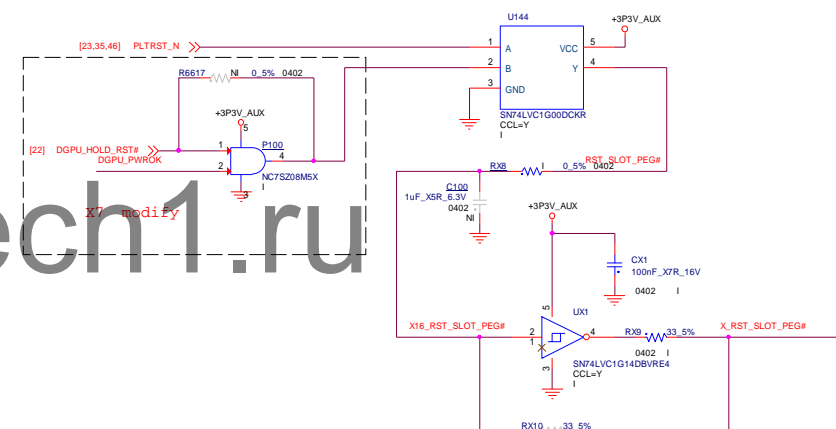
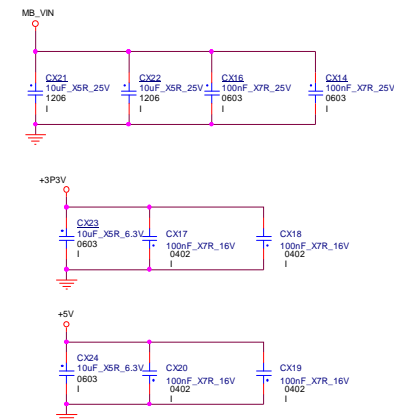
If swap SPD from A4 to A2: cut R844,R843 connect M_DIMM3_SA1 to GND, connect M_DIMM3_SA0 to DIMM_VDDSPD

SPD ADDRESS: 001
SMBUS ADDRESS: A2

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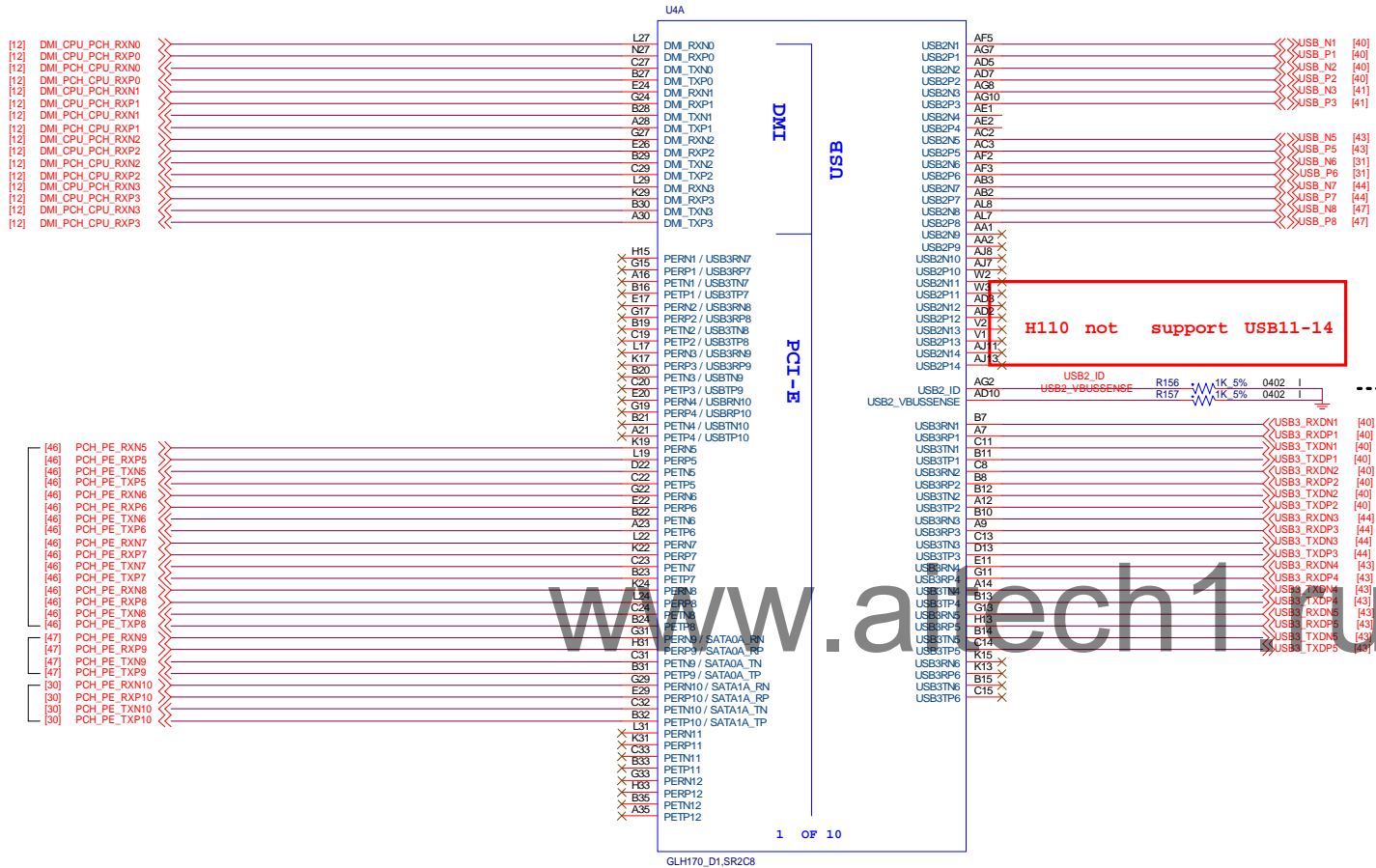
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|-------|--------------|
| Title | GFX M.2 SLOT |
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| | |
|-----------------------------|----------------|
| Date: Monday, June 13, 2016 | Sheet 18 of 70 |
|-----------------------------|----------------|

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| Custom | Tesla | | | | X9 |
| Date: Monday, June 13, 2016 | | Sheet | | 19 | of 70 |



- REAR USB 3.0
- Internal USB 2.0 Dongle
- REAR USB 3.0 Type-C
- Card Reader
- Front USB 2.0
- M.2

H110 not support USB11-14


Only USB2 port1 and USB3 Port1 can support On the go function
USB ID and USB VBUS sense are for OTG function.
Follow USB to add PU with 1kOhm.

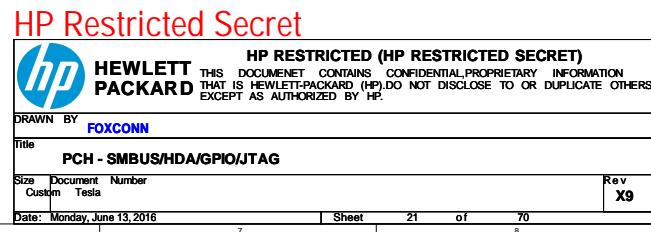
REAR USB 3.0 (1-2)

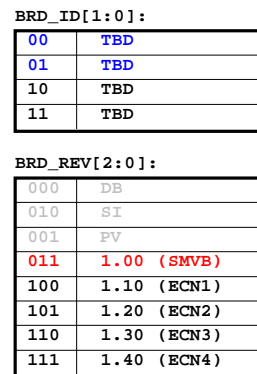
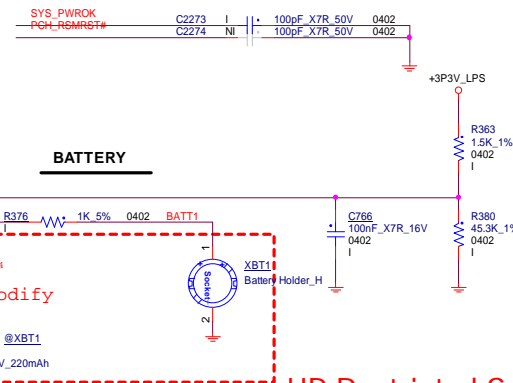
FIO USB 3.0

REAR USB 3.0 Type C


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| Custom | Tesla | | | | X9 |
| Date: Monday, June 13, 2016 | | Sheet | | 20 | of 70 |

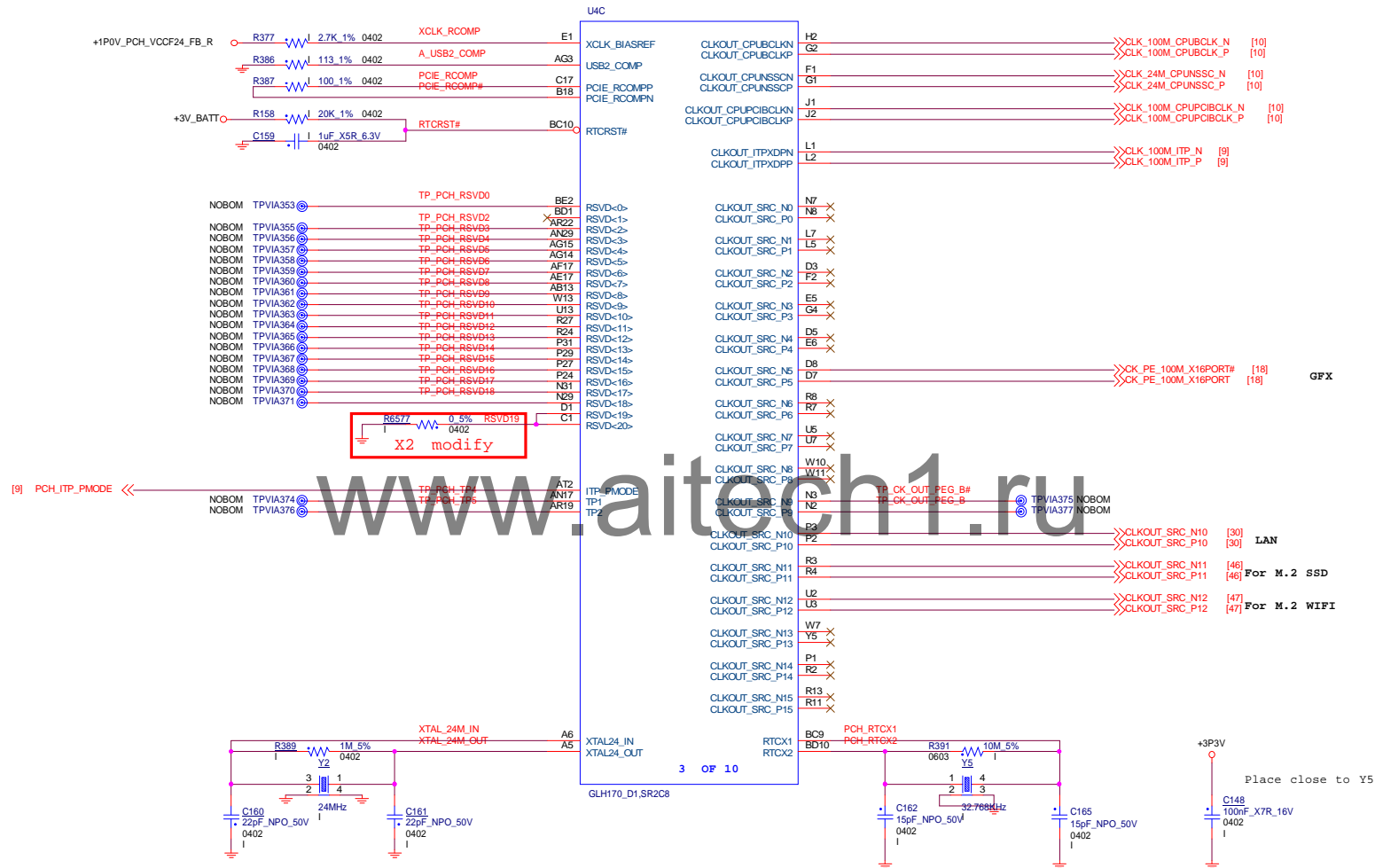


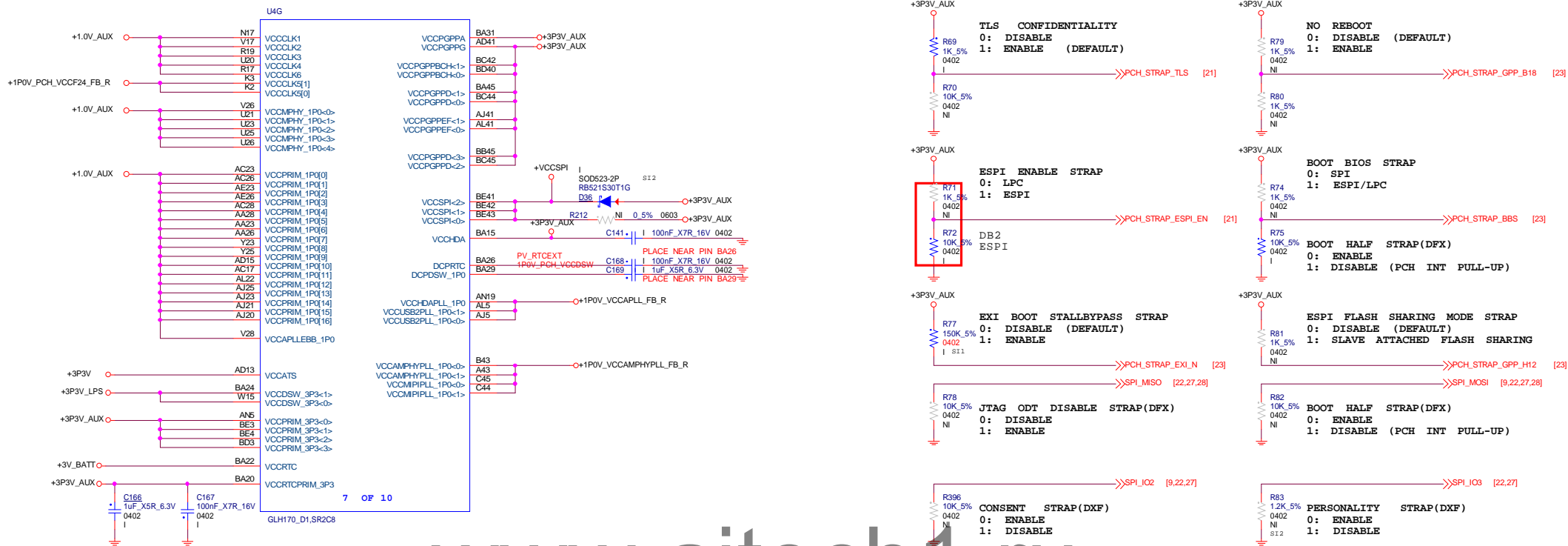


BATTERY

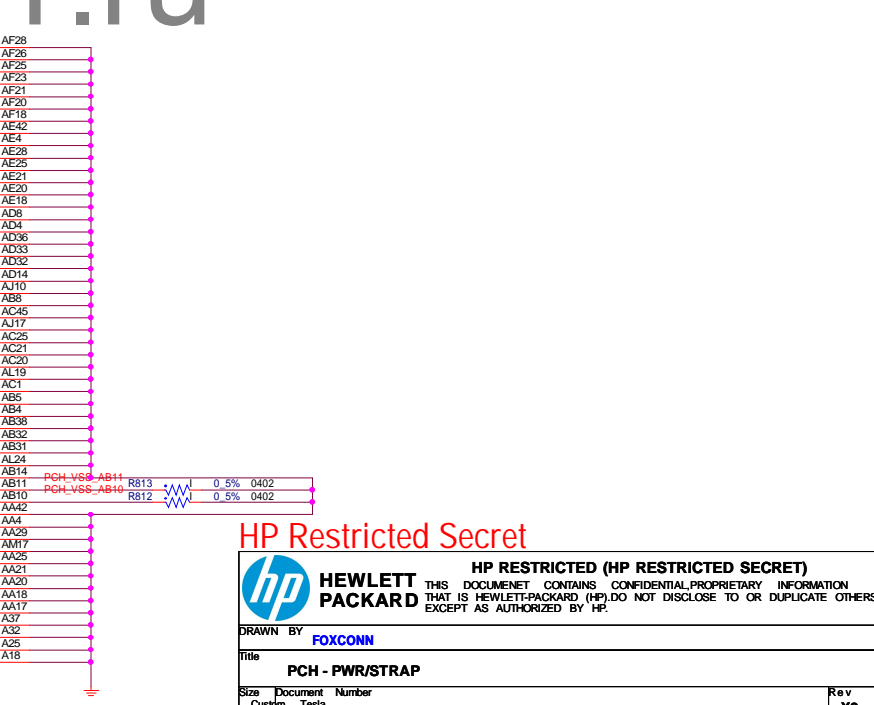
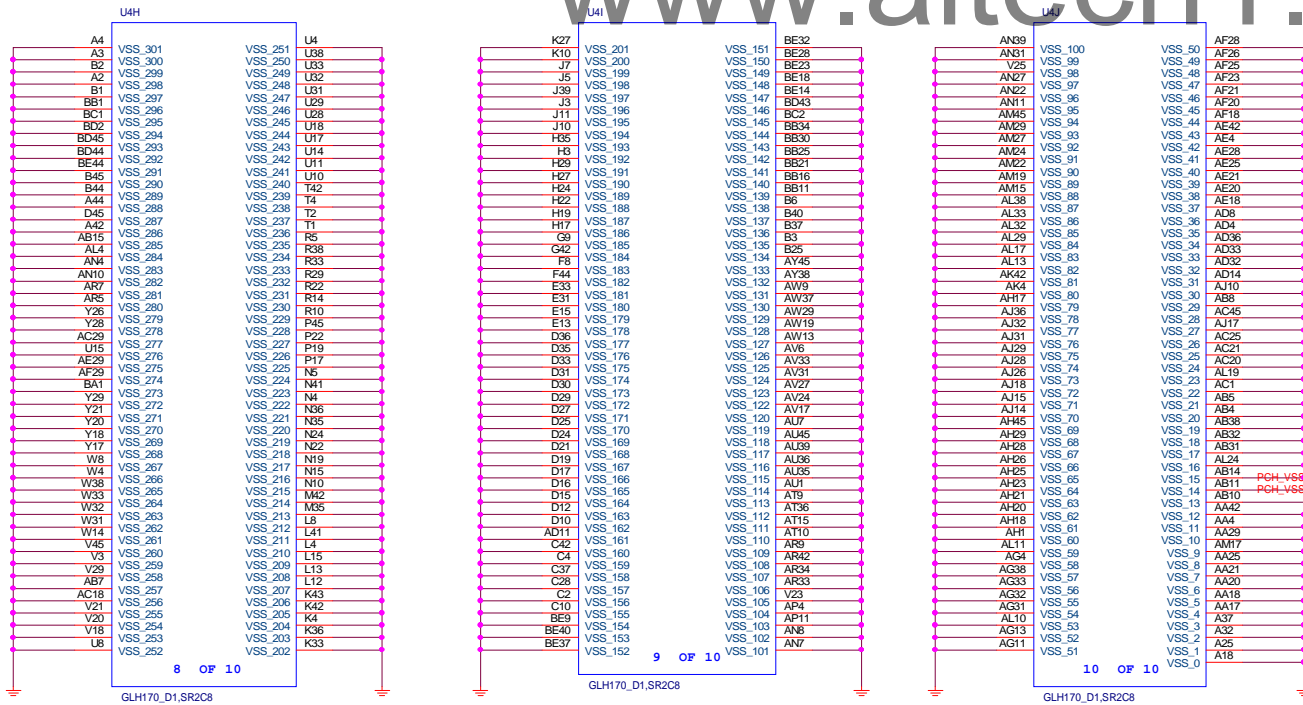
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PCH - CLOCK DISTRIBUTION





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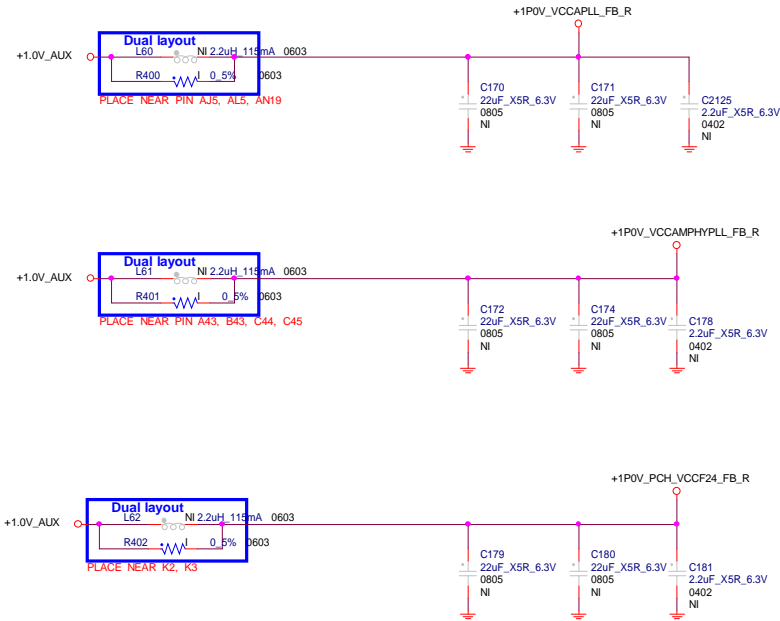


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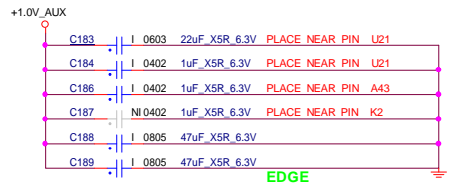
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SKYLAKE Decoupling & filter

FILTER



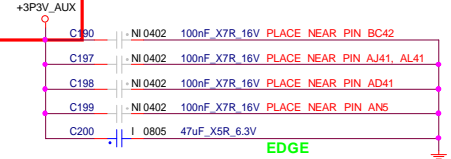
V1.0A



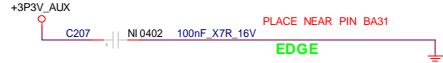
V3.3 DSW



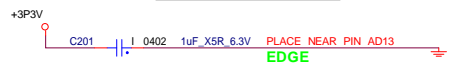
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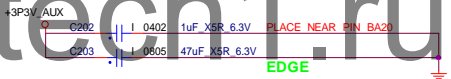
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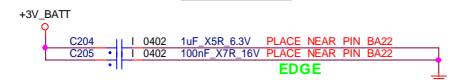
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC



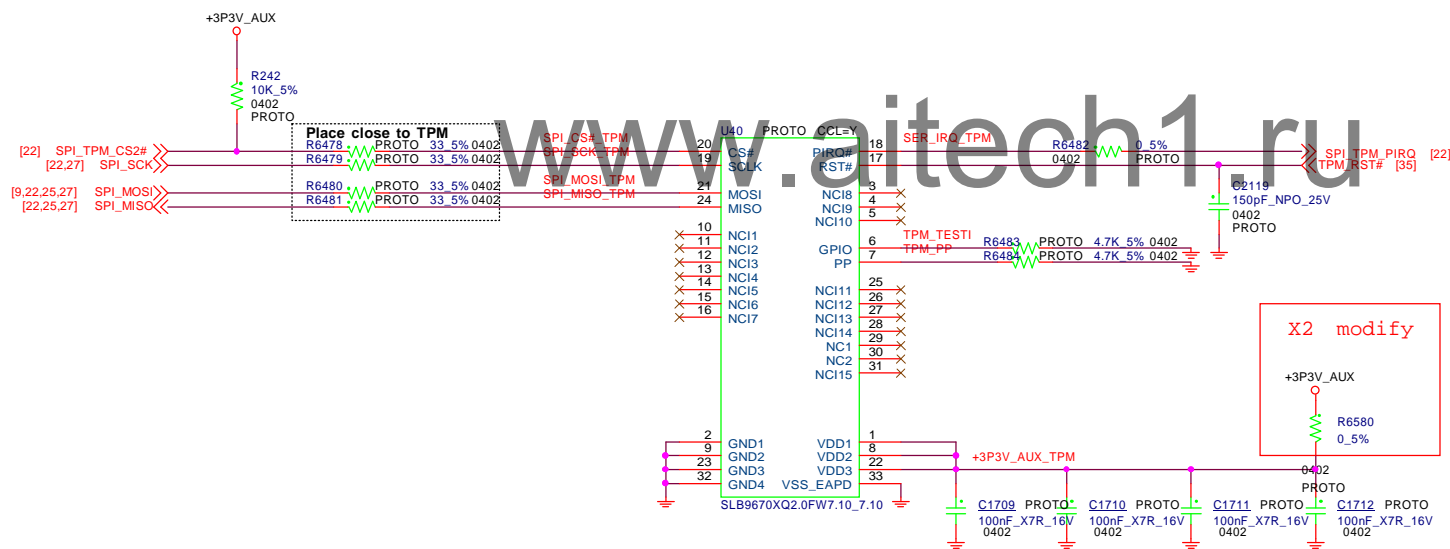
Power Plane Isolation

Need to update for SLK


| Voltage | Interface | PCH Pins sharing power rail |
|------------------------|--------------------|--|
| VCC_PCH 1.05V | Core | U26, U25, U23, U21, V26, |
| | PCIe/SATA/ USB3 | T19, T20, P22, P23, P25, P26, P28, P14, P16, P17 |
| | GPIO/LPC | AC12 |
| | FDI | M14 |
| | DIFFCLK | U12, V14 W14 AB2 |
| | SSC | T16, V16 AA16, W16 |
| | USB2 | AF19, AF20, AF22, AF23, AP22 |
| PCH 3.3V Standby | SUS | AM33, AN33 |
| | USB2 | AH18, AH20, AH22, AJ20, AK20 |
| | AZALIA | AW26 |
| | USB3 | P20 |
| | RTC | AP35 |
| PCH 3.3V | CLK | AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11, |
| | HVCNOS | AG1 |
| | PCIe | AV3, AW3 |
| | Core | U30, W30 |
| | Fuse | AF26 |

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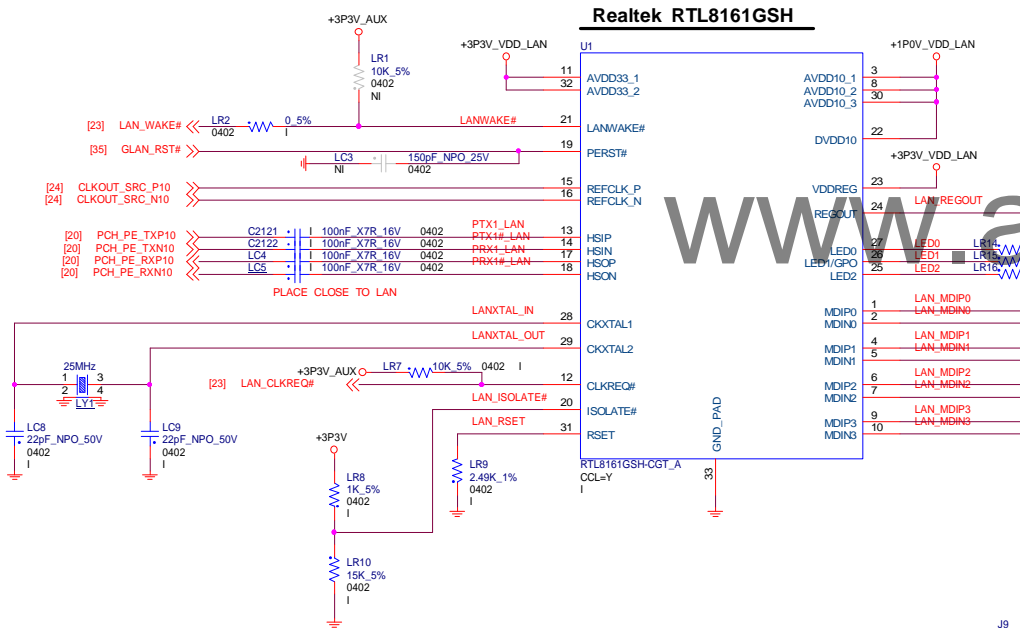
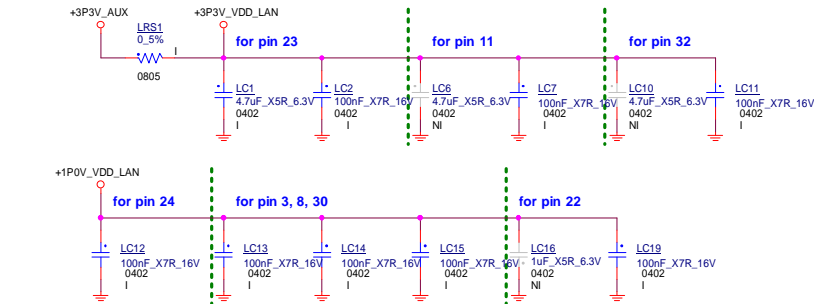
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RTL8161GSH

RTL8161GSH: Switching Regulator Inside
RTL8161GH: LDO Regulator Inside

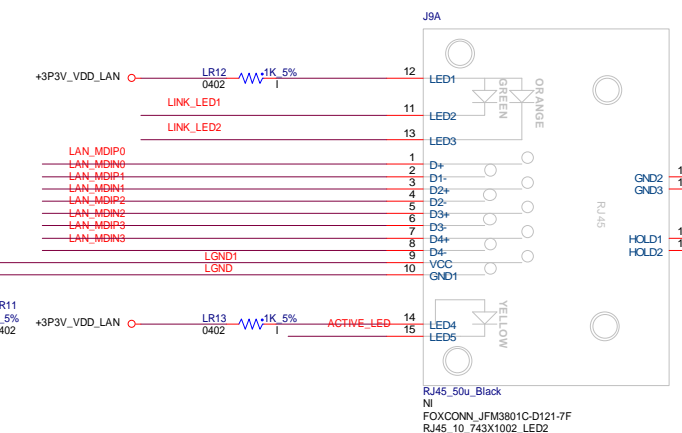


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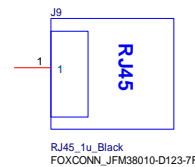
X5 modify CO-LAY

Power Consumption of these modes will be reduced by 0.15mA @ 3.3V with L1 OFF supported.

| | mA@3.3V | mW @ whole LOM |
|--------------------------------|---------|----------------|
| 10M (idle)* | 8.44 | 27.85 |
| 10M (TxRx) | 67.57 | 222.98 |
| 100M (EEE)* | 14.06 | 46.4 |
| 100M (idle, >30m)* | 37.85 | 124.91 |
| 100M (idle, <30m)* | 34.93 | 115.27 |
| 100M (TxRx, >30m) | 63.95 | 211.04 |
| 100M (TxRx, <30m) | 61.41 | 202.65 |
| 1000M (EEE)* | 14.49 | 47.82 |
| 1000M (idle, >30m)* | 100.53 | 331.75 |
| 1000M (idle, <30m)* | 84.15 | 277.70 |
| 1000M (TxRx, >30m) | 128.85 | 425.21 |
| 1000M (TxRx, <30m) | 112.08 | 369.86 |
| ALDPS* | 3.80 | 12.54 |
| S3/S5 enable WOL (link@10M) | 8.27 | 27.29 |
| S3/S5 disable WOL | 0.45 | 1.49 |
| Lan Disable Mode | 0.45 | 1.49 |



EOS, Line to Line 1KV, Line to ground 4KV
ESD, +/- 8KV by contact, +/- 15KV by air discharge

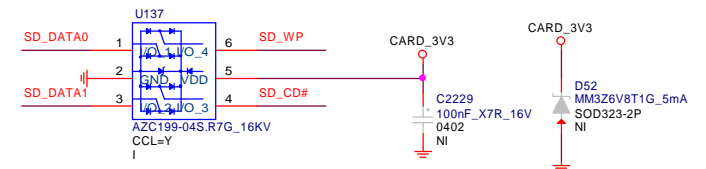
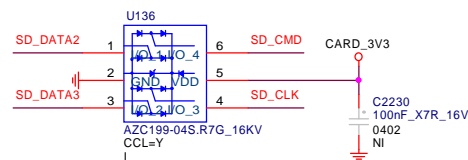
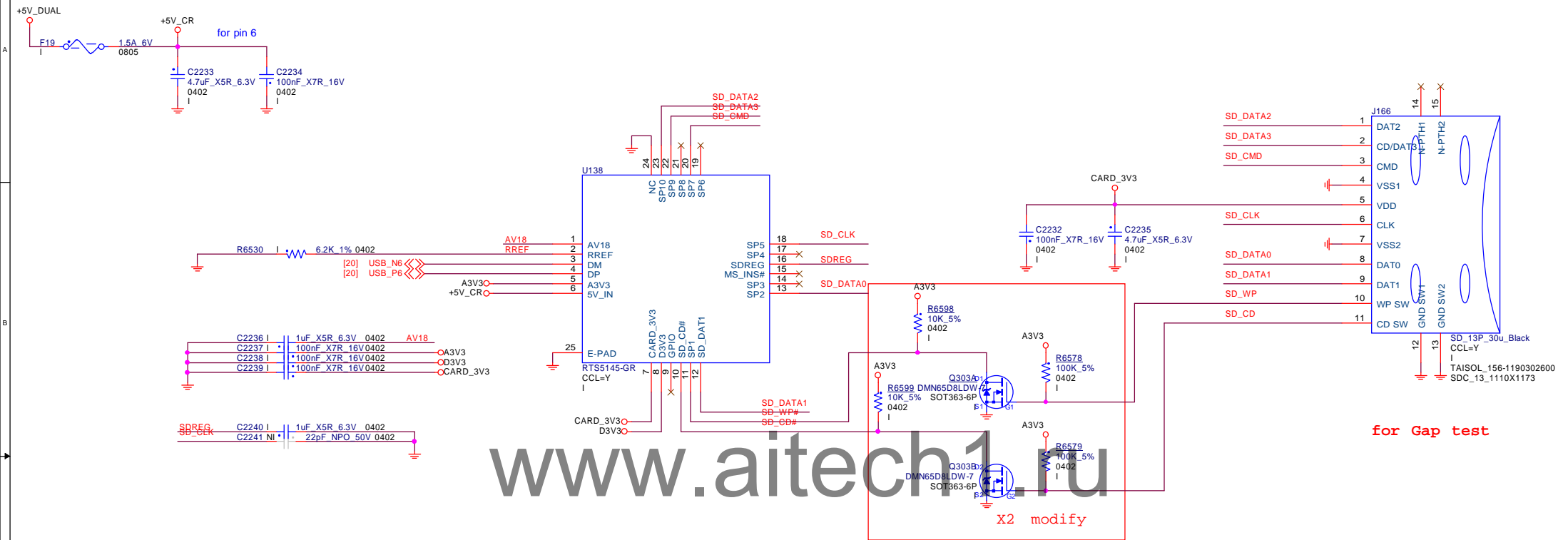


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CARD READER



| Measurement items | Current Value | Spec Requirement |
|----------------------------------|---------------|------------------|
| Unconfig. Current of L0 | 35 mA | < 150mA |
| Config. Current of L0 | 40 mA | < 500mA |
| LPM L1 State | 40 mA | <500mA |
| L2(Suspend) State | 250uA | <2.5mA |
| Delink State(Card not presented) | 85uA | < 2.5mA |

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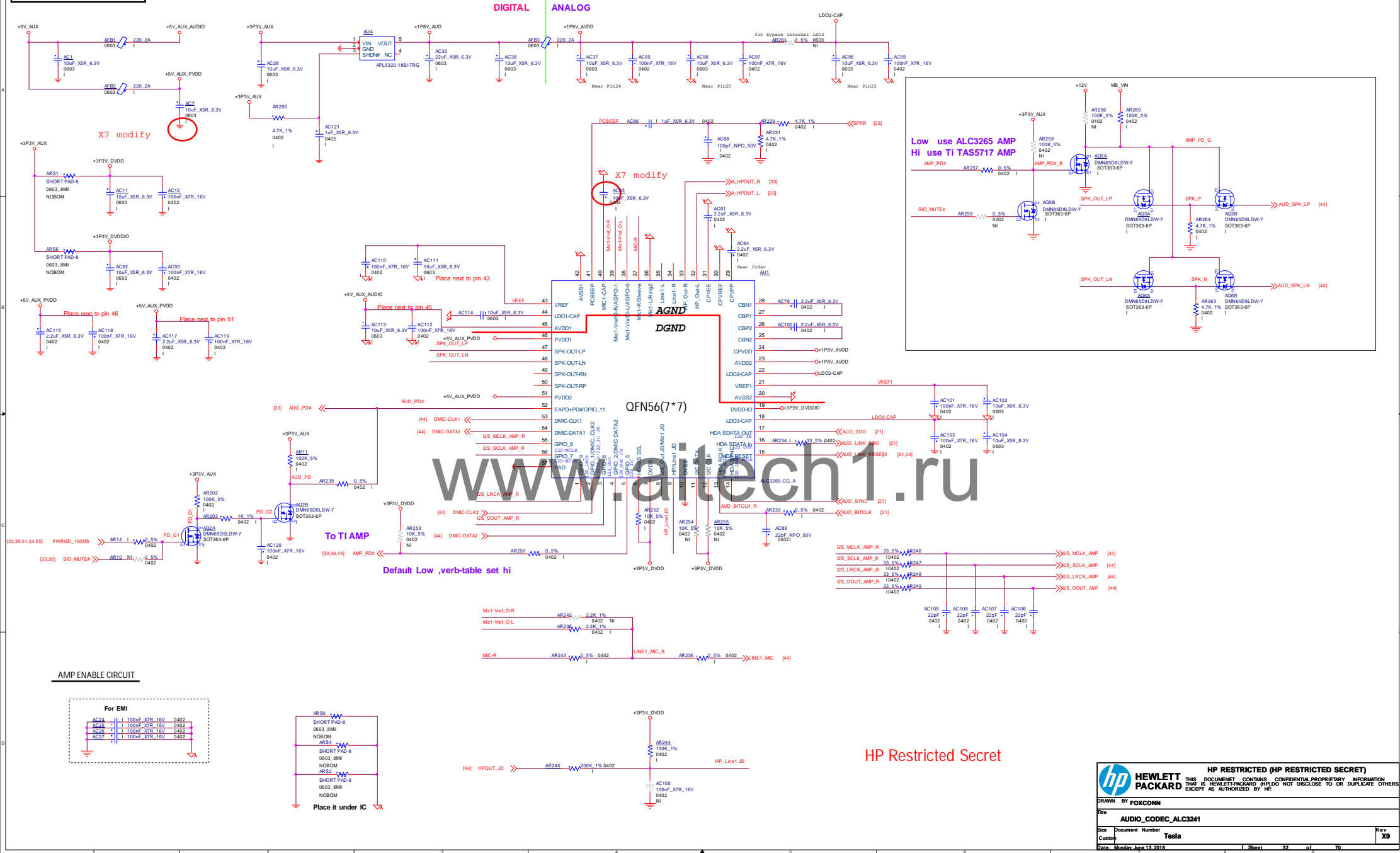
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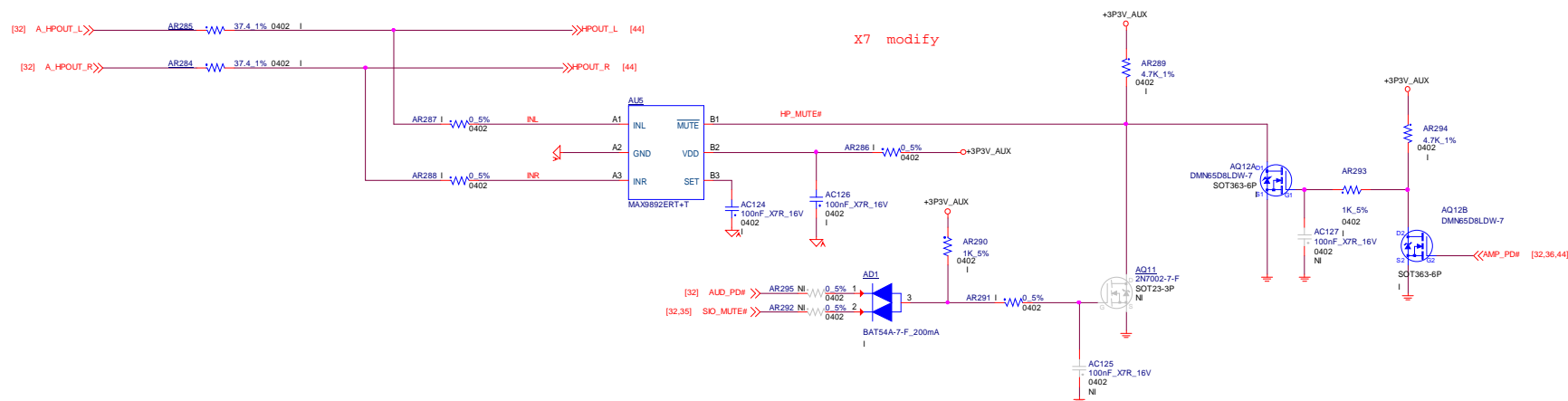
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AUDIO ALC3265



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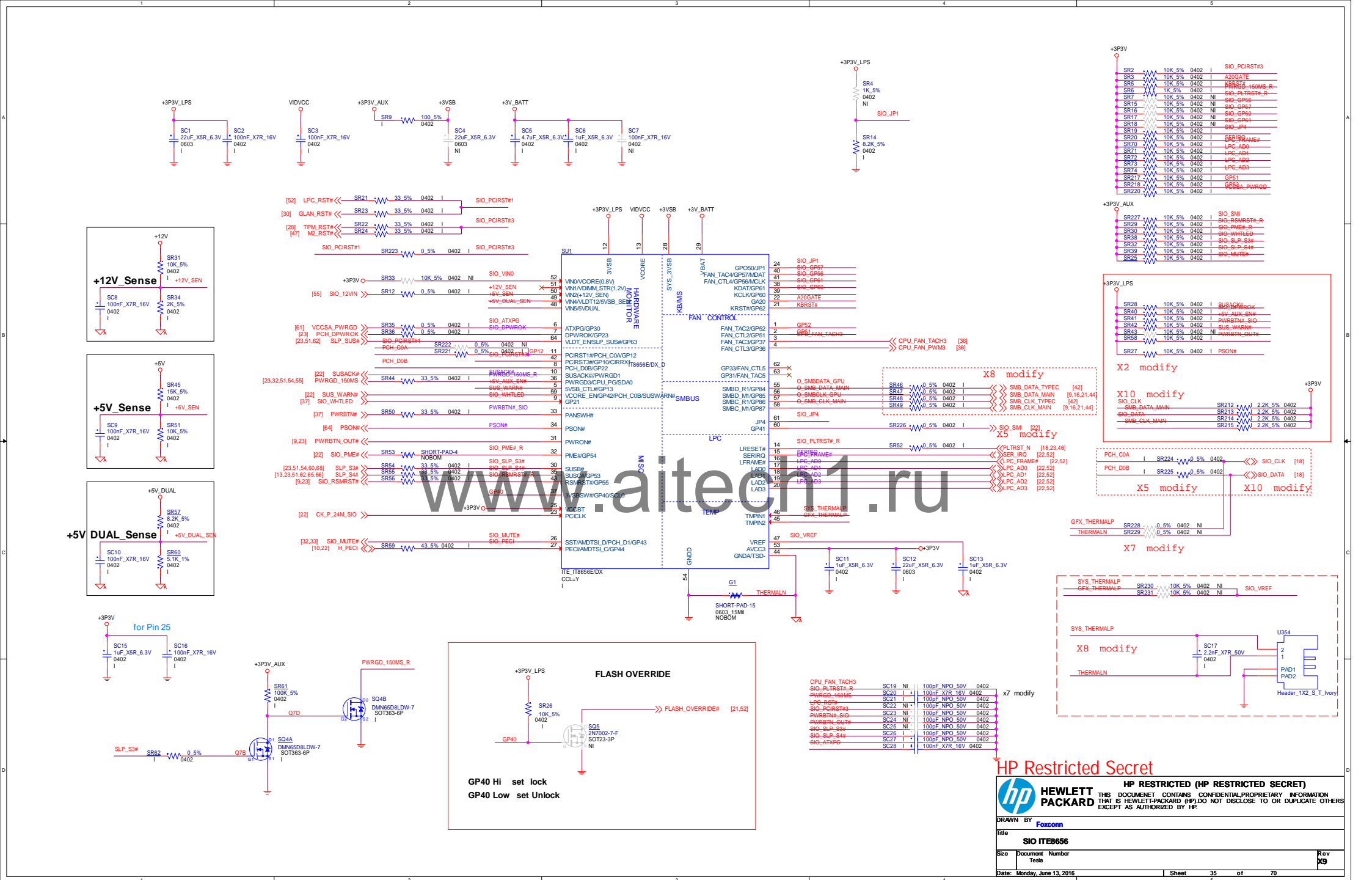


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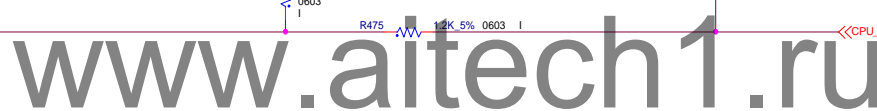
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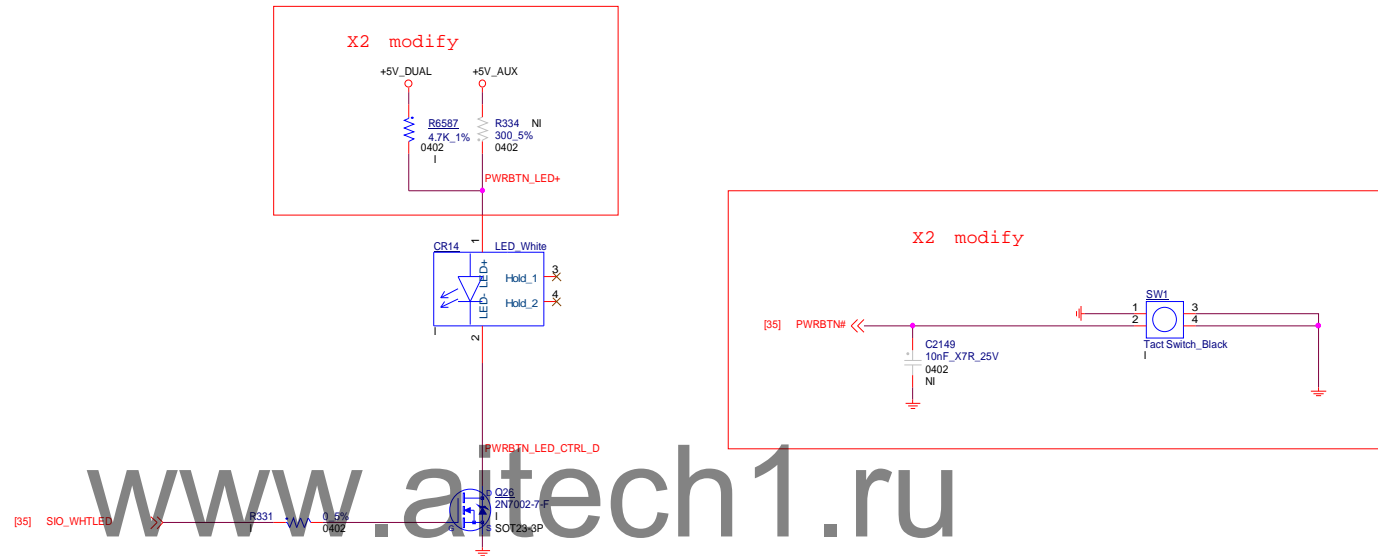
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Color: Ivory




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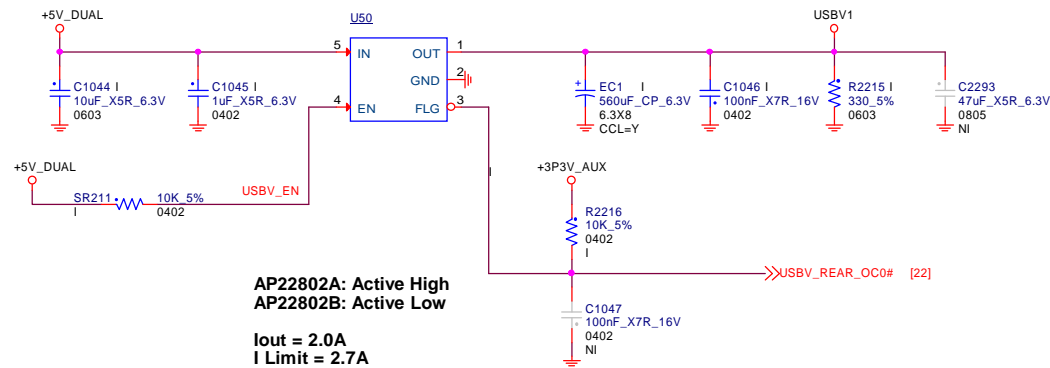
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USB 3.0 Power


REAR USB 3.0 *2 PWR

(Height Limitation : 13-mm)



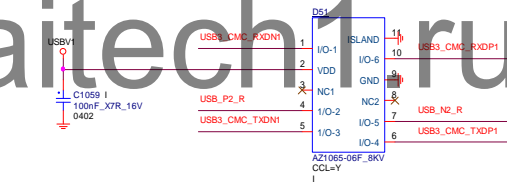
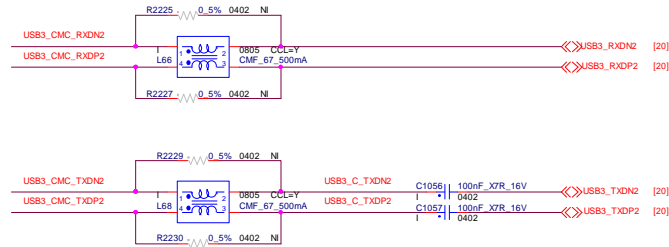
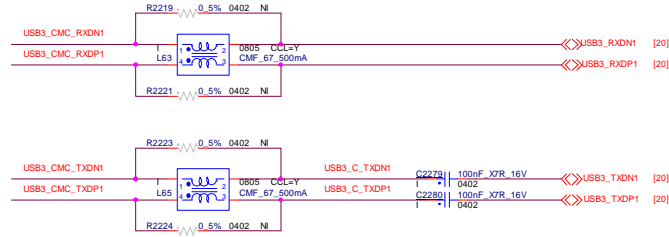
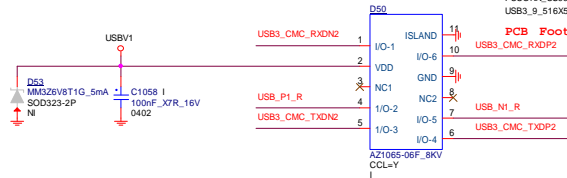
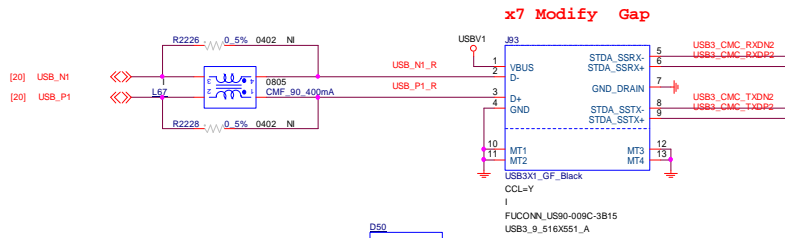
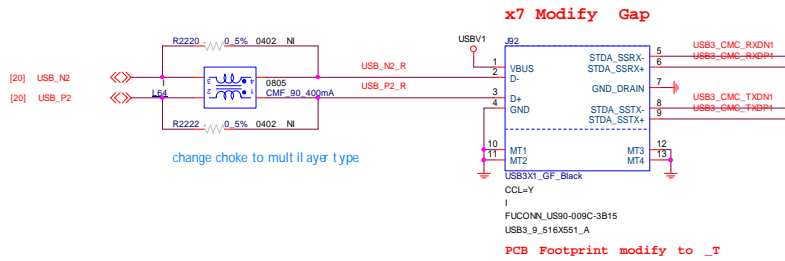
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USB 3.0 CONN

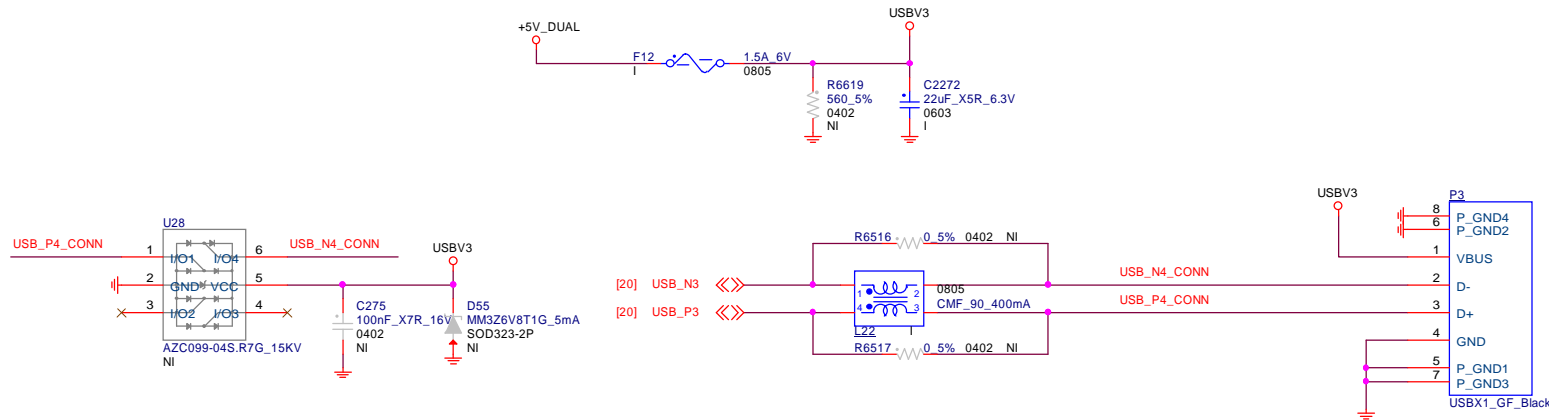
Rear USB3.0 x3



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| C | Petra - Lucky | | | | X9 |
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INTERNAL USB2.0 CONN. (WIRELESS KB/MS DONGLE)

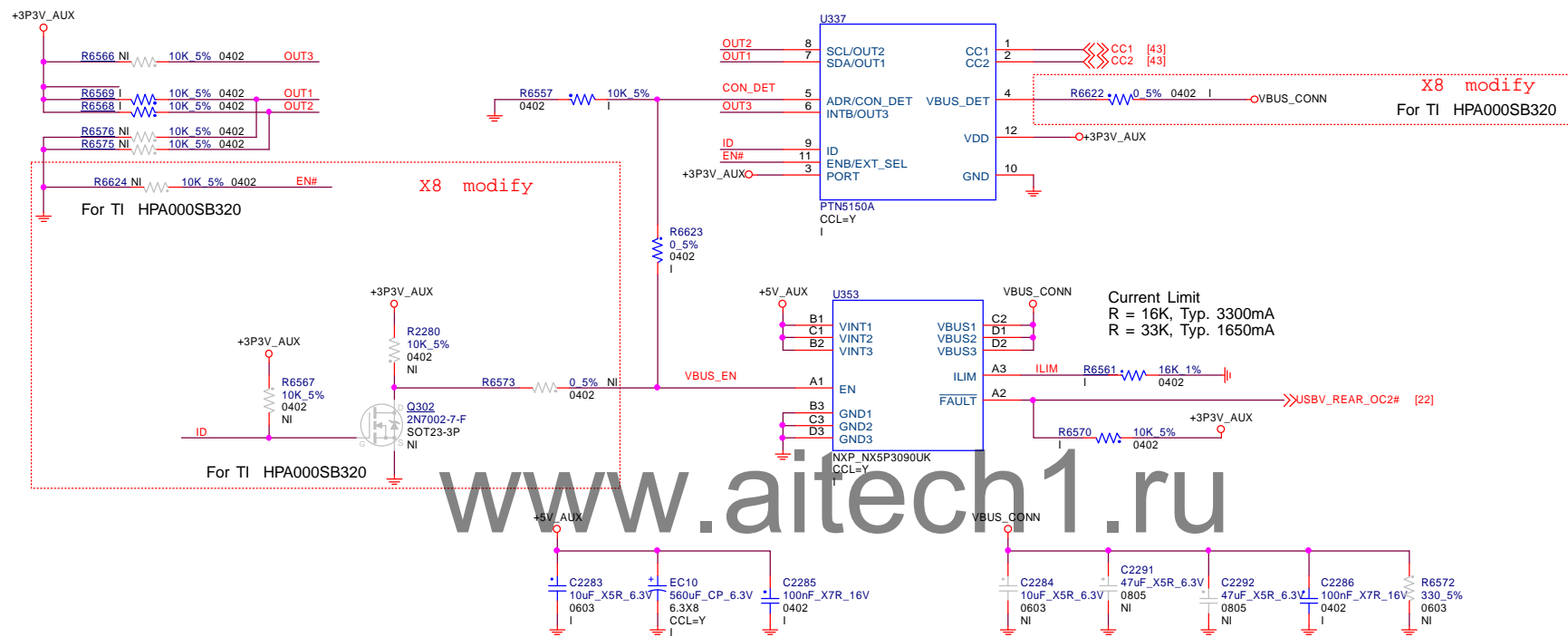


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for colay USB header

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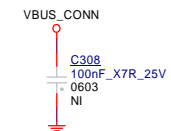
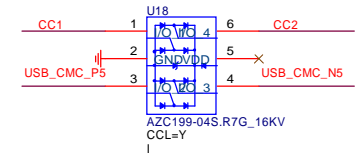
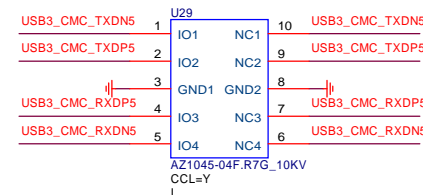
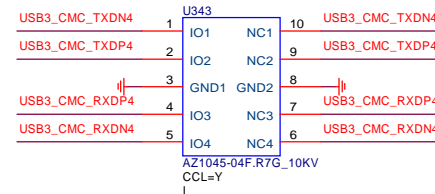
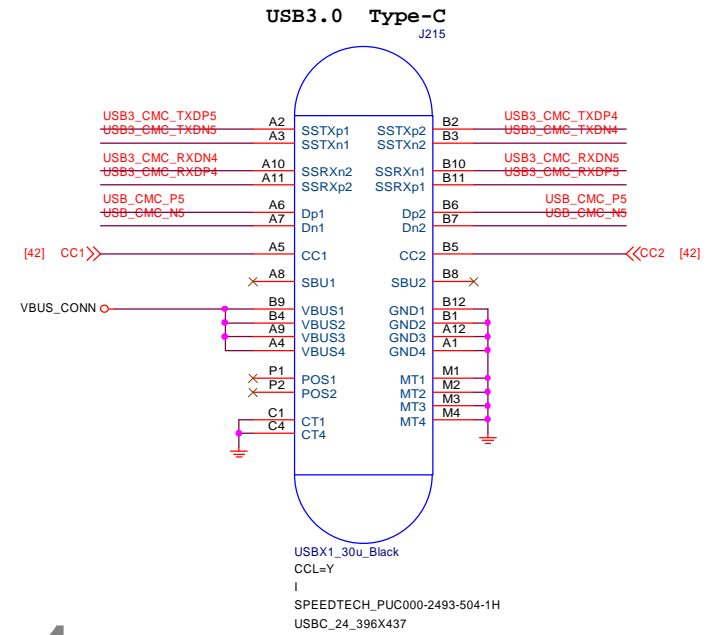
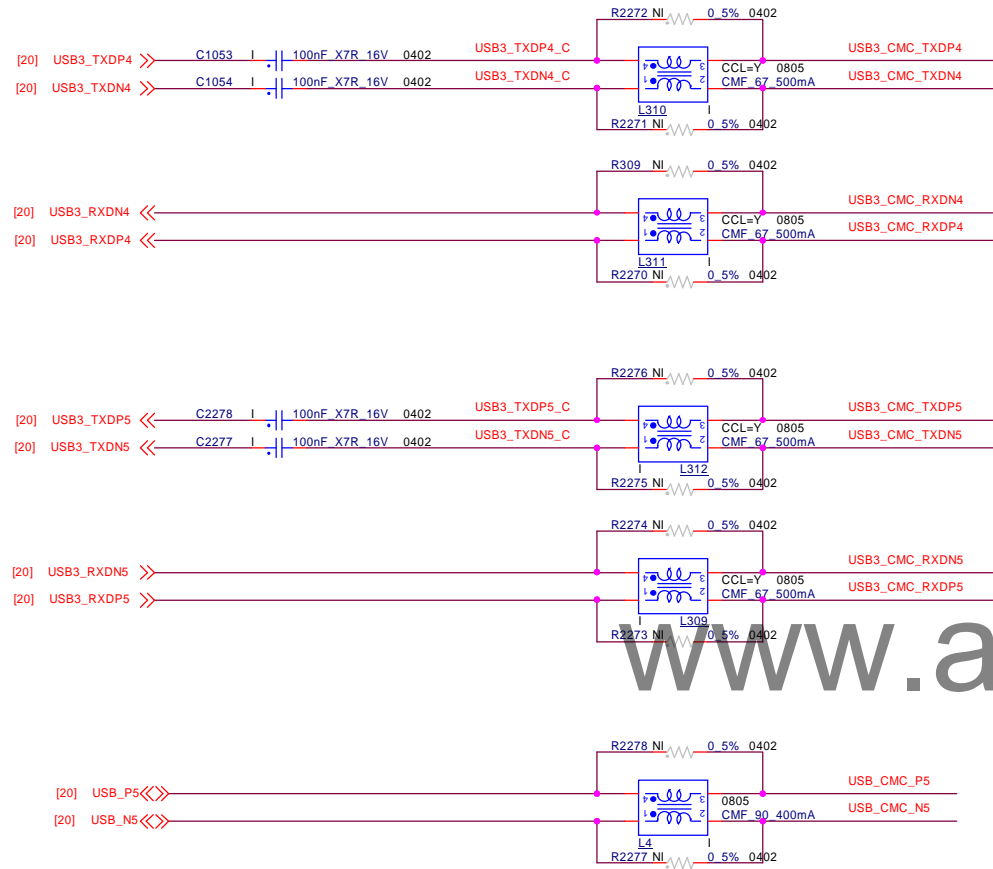
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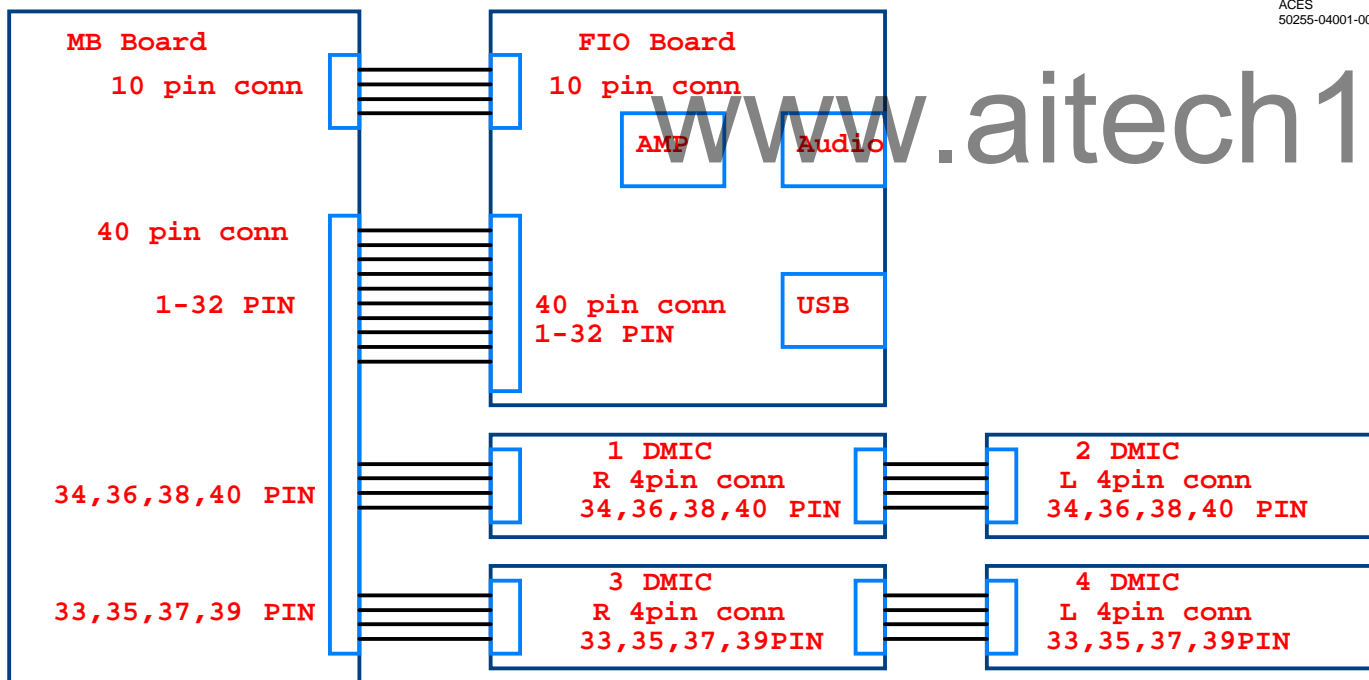
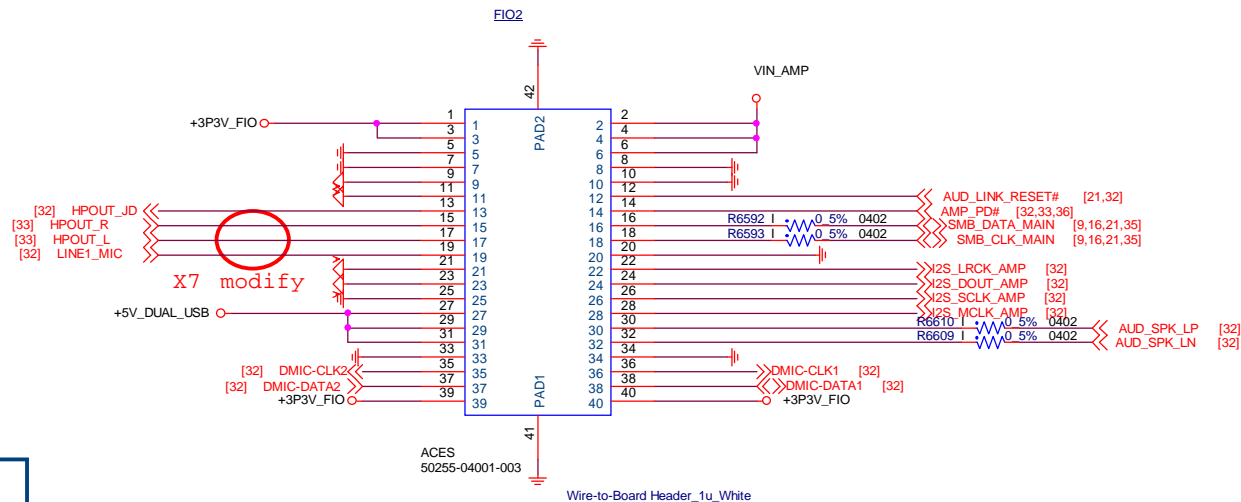
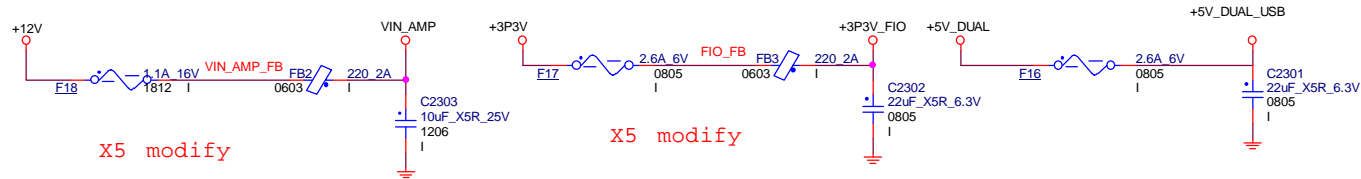
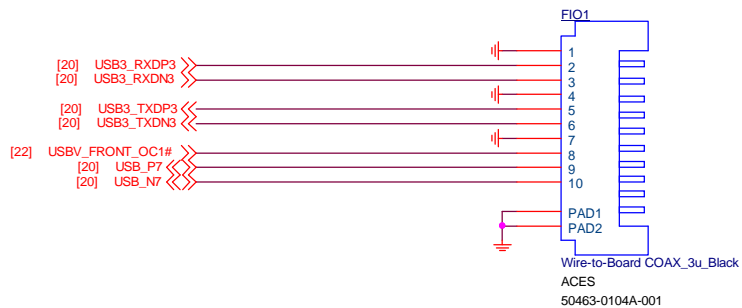
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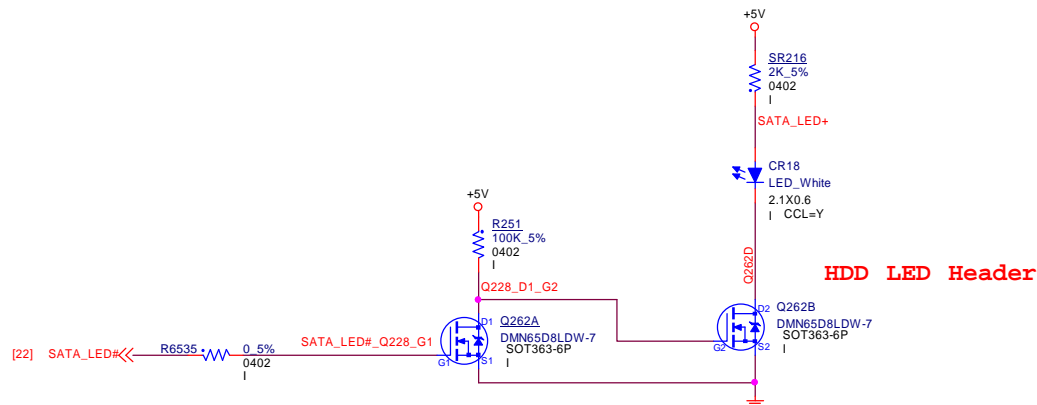
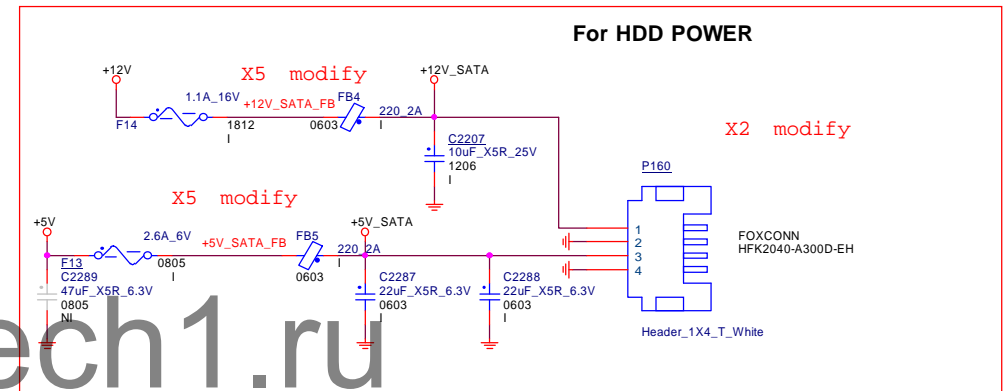
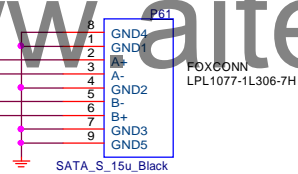
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[22] SATA_TXN0 C2200 NI 10nF X7R 25V 0402
[22] SATA_RXN0 C2201 NI 10nF X7R 25V 0402
[22] SATA_RXP0 C2202 NI 10nF X7R 25V 0402


X5 modify

SERIAL ATA 0
HDD Blue

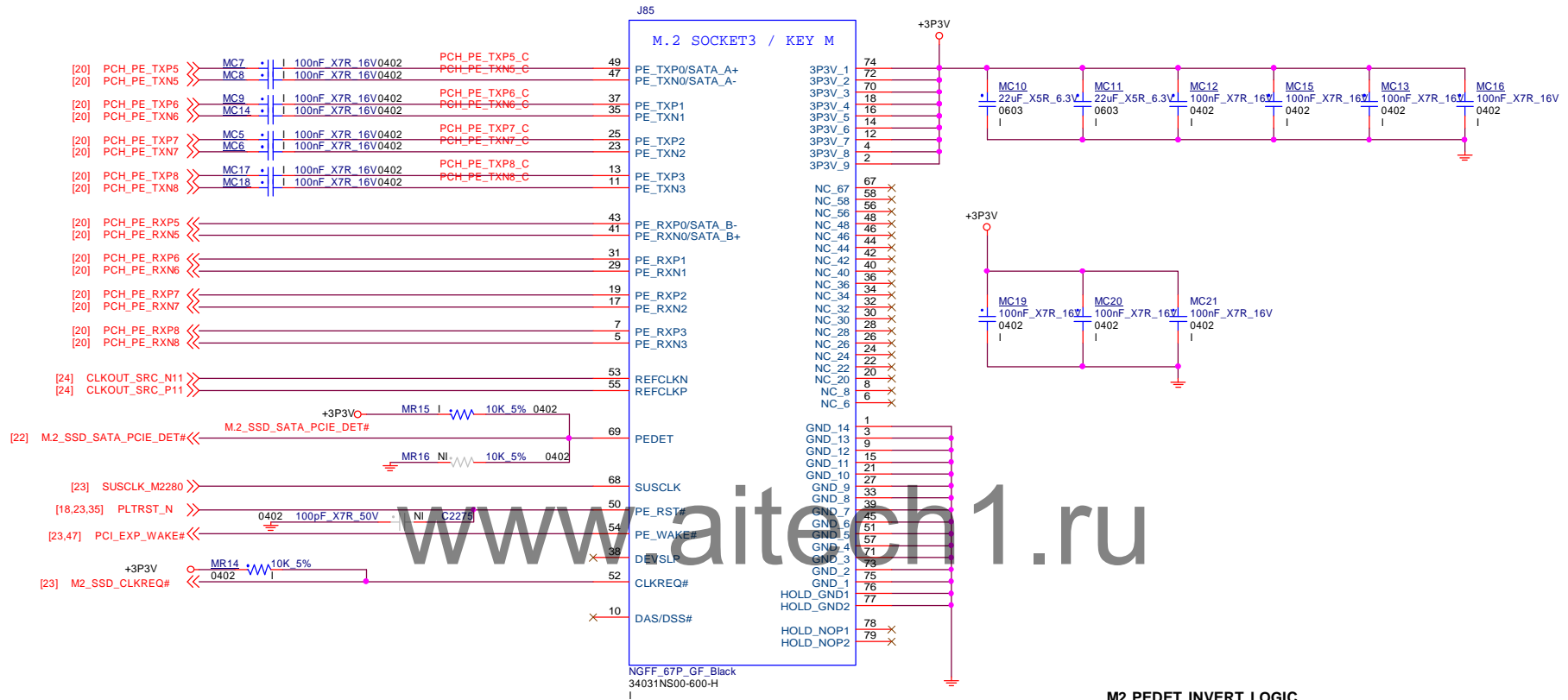
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| Date: Monday, June 13, 2016 | | | Sheet | 45 of 70 | |

M2. 2280 - STORAGE



M2 PEDET INVERT LOGIC

INVERT LOGIC AS PER SATAE REQUIREMENT FOR M.2 SSD
MOUNT ZR10 AND UNMOUNT ZU101
IF INVERT LOGIC IS NOT USED

M2.2280

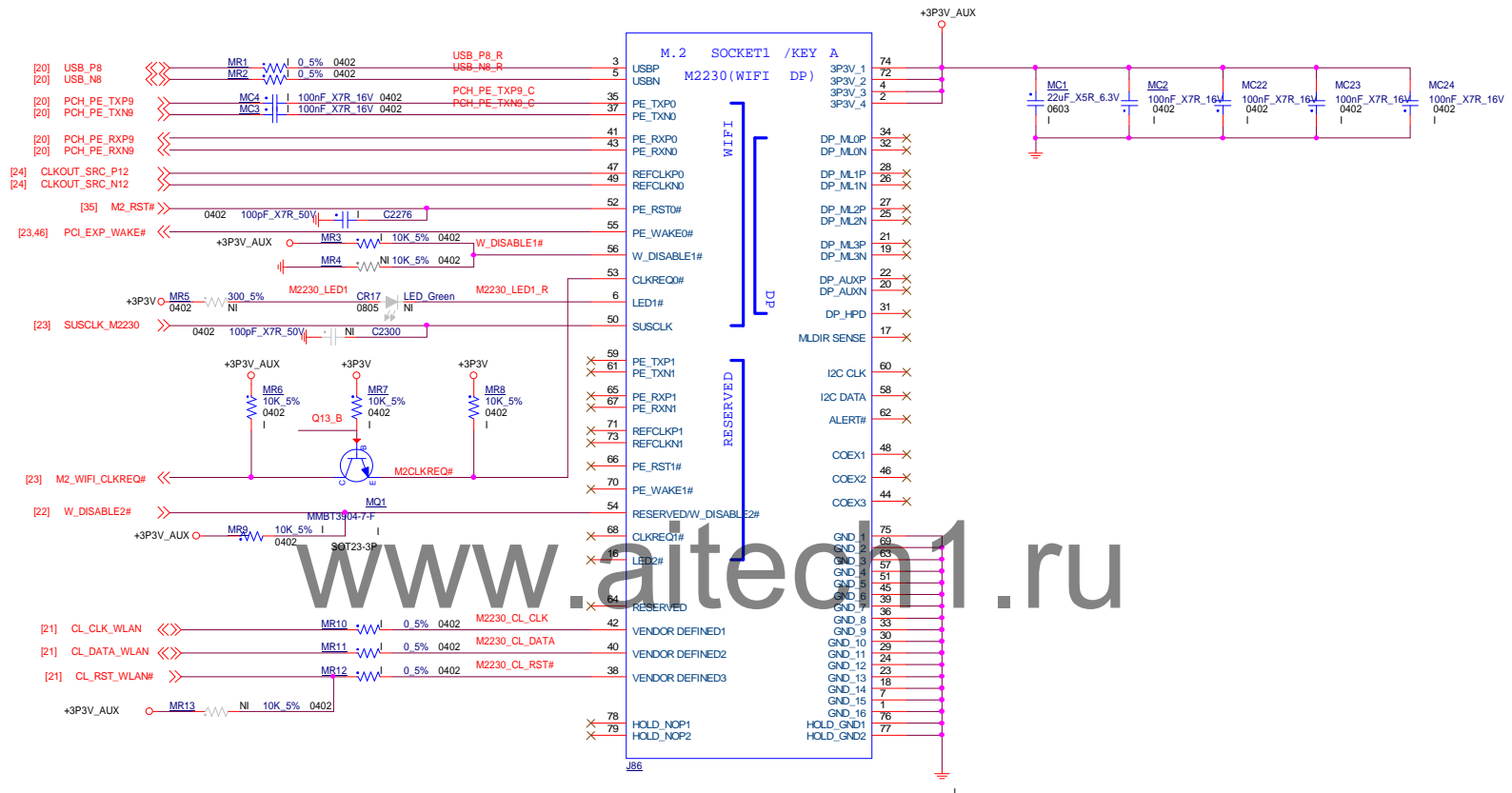


NUT2
Screw_4.5

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| Title M2_2280_SSD | | | | | |
| Size | Document Number | Rev | | | |
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M2. 2230 - WLAN



NUT1
Screw_4.5

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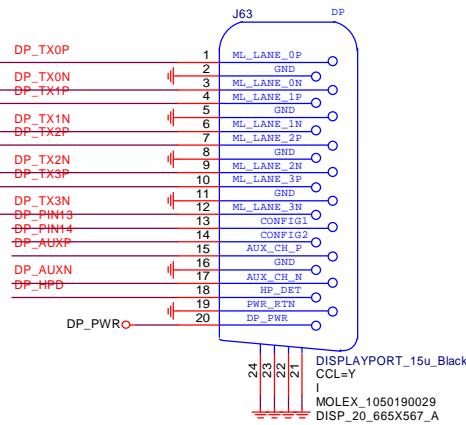
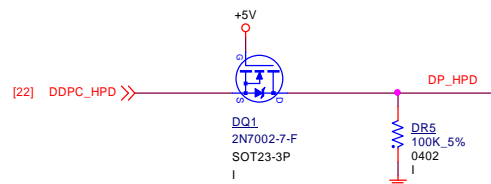
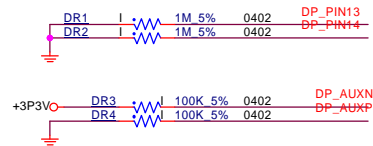
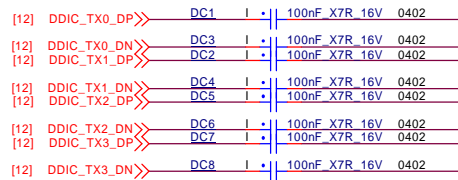
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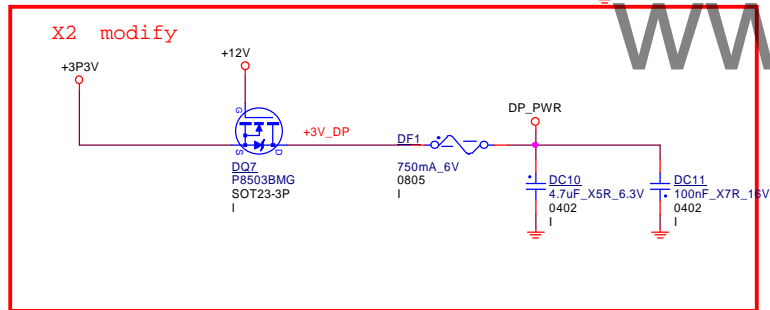
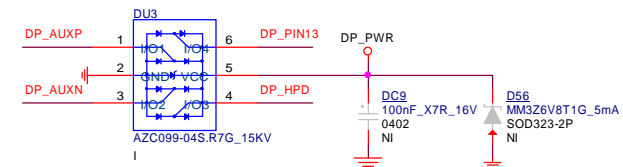
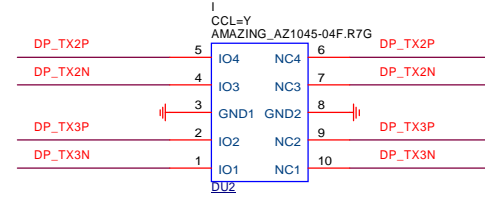
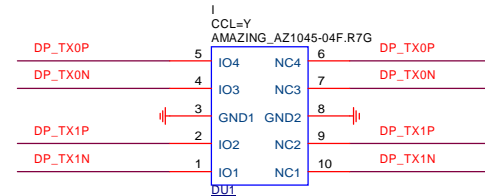
Date: Monday, June 13, 2016

Sheet 47 of 70

Rev
X9

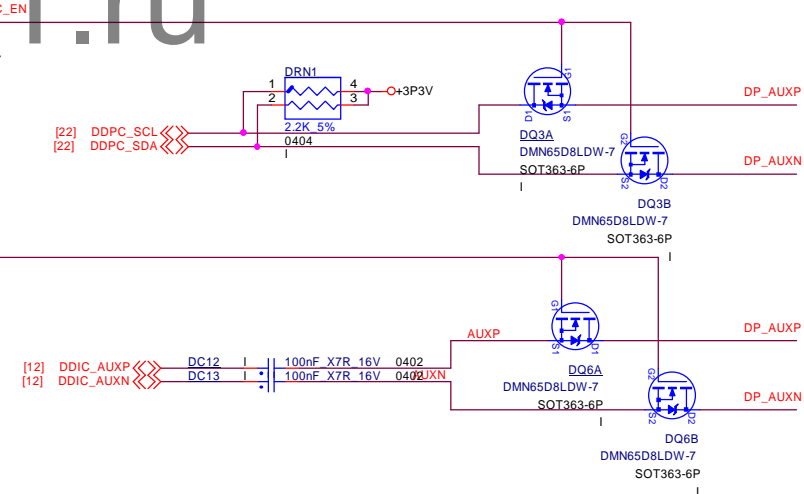
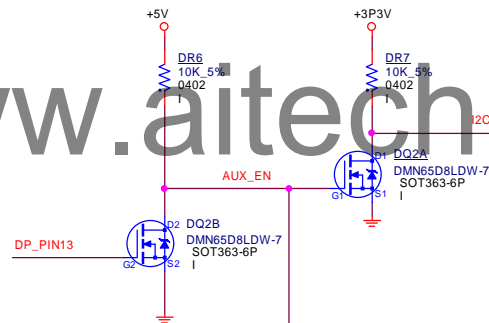


for Gap test



PDG p.137

| PIN13 | | FUNCTION |
|-------|--------|-------------------|
| DP | DONGLE | |
| L | X | DEVICE_C_DETECT |
| X | H | DEVICE_C_DETECT_N |



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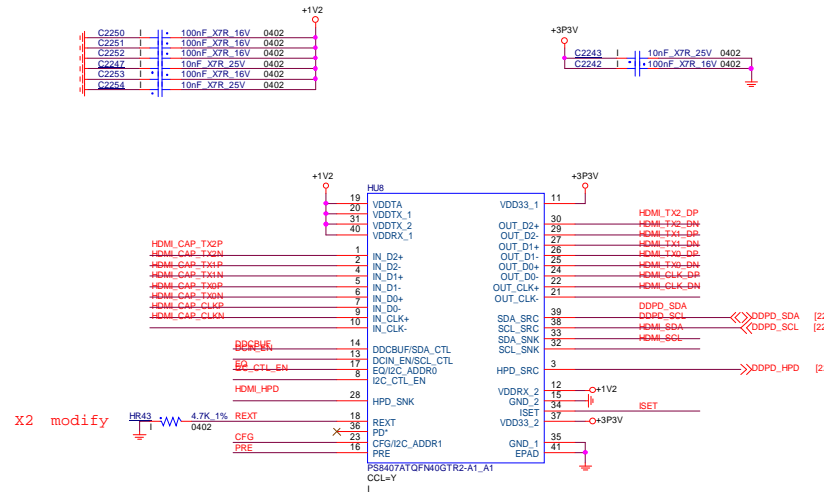
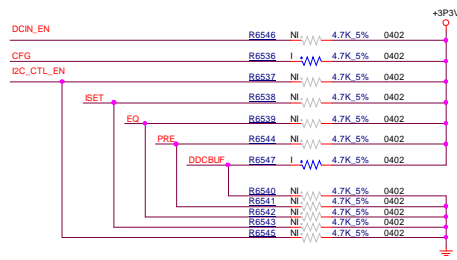
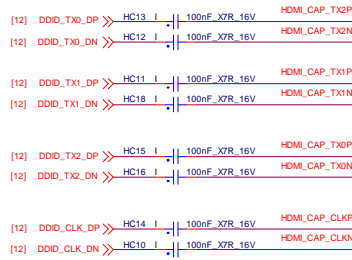
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| Custom | Tesla | | | | |
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| | | | | | Rev X9 |

Audomatic POWER Down

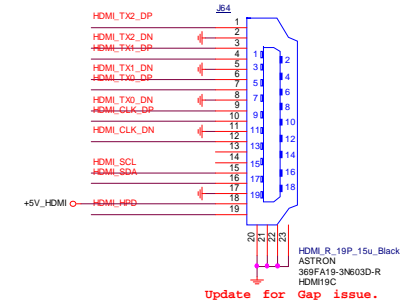
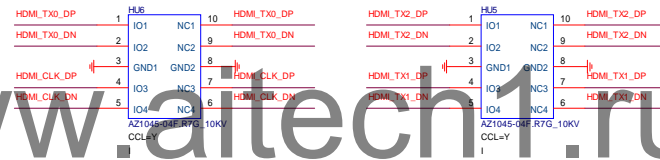
$$1.2V \ 37\mu A = 44.4\mu W$$

$$3.3V \ 28\mu A = 92.4\mu W$$

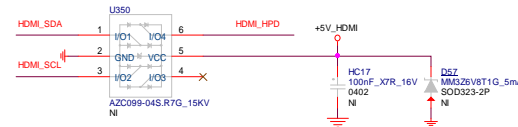
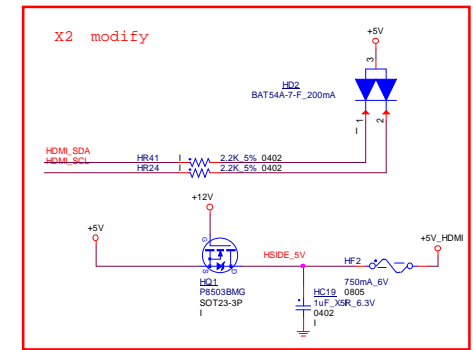
$$\text{Total} = 136.8\mu W = 0.14mW$$



X2 modify



Update for Gap issue.




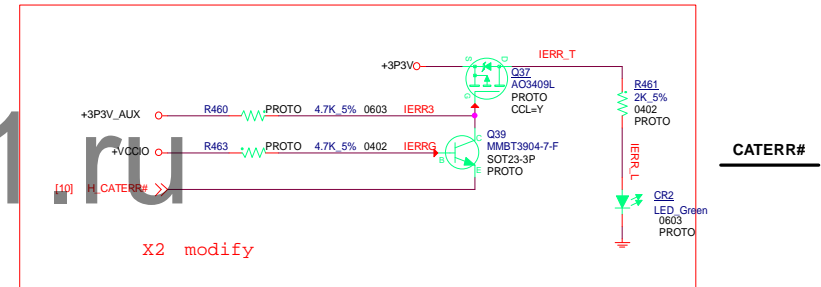
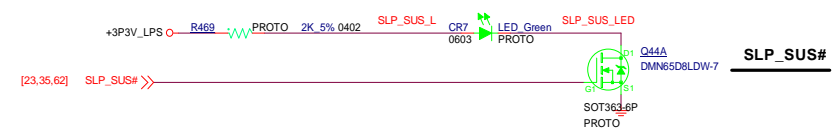
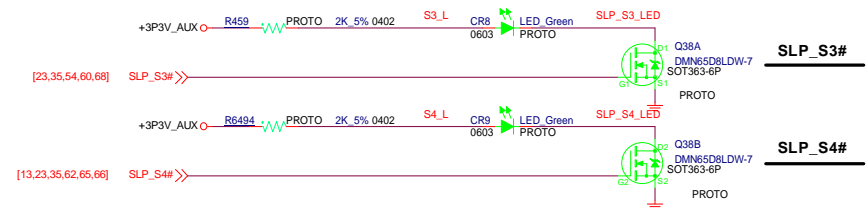
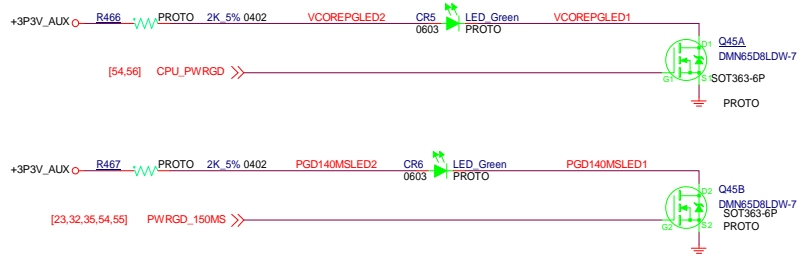
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| Title: HDMI PORT | | | |
| Size: C | Document Number: Tesla | Rev: X9 | |
| Date: Monday, June 13, 2016 | | Sheet: 49 | of: 70 |

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| Title BLANK | | | | | |
| Size A | Document Number Tesla | | | | Rev X9 |
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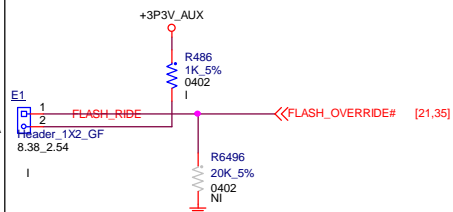


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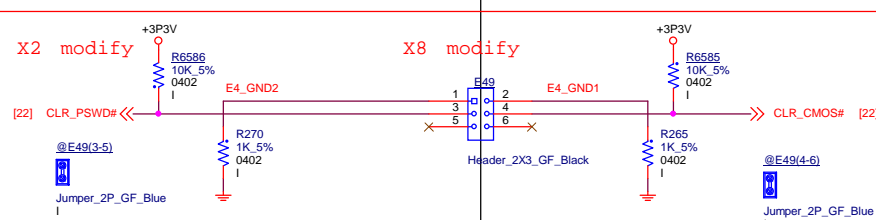
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| Title LEDs/HOODLOCK_SENSE | | | |
| Size | Document | Number | Rev |
| Custom | Tesla | | X9 |
| Date: Monday, June 13, 2016 | | Sheet | 51 of 70 |

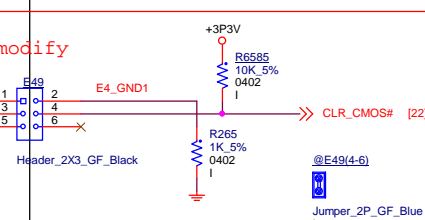
FLASH OVERRIDE



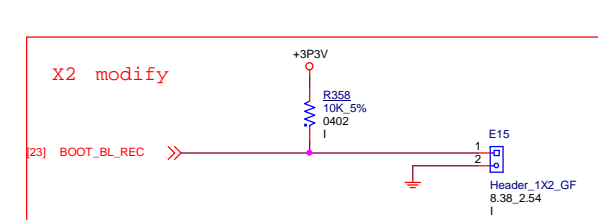
CLEAR PASSWORD



CLEAR CMOS



BOOT BLOCK RECOVERY

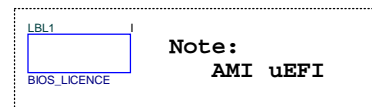


HOOD SENSE CIRCUIT

Have to take care the location



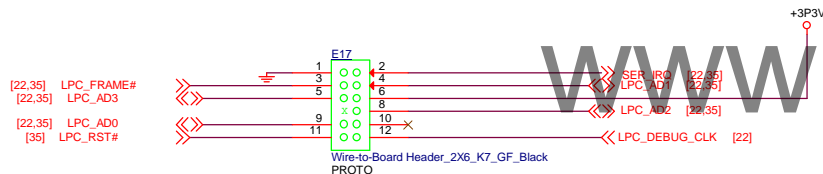
Licence Label



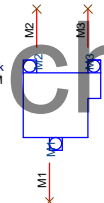
PCB

PCB1
Printed Circuit Board
PCB_0101CFC07-575-G
CCL=Y

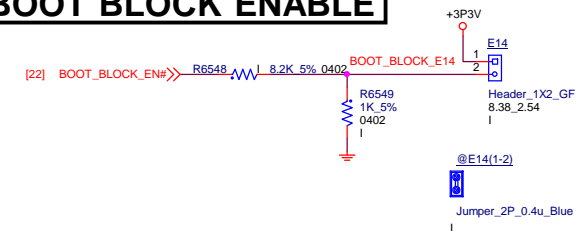
LPC DEBUG PORT



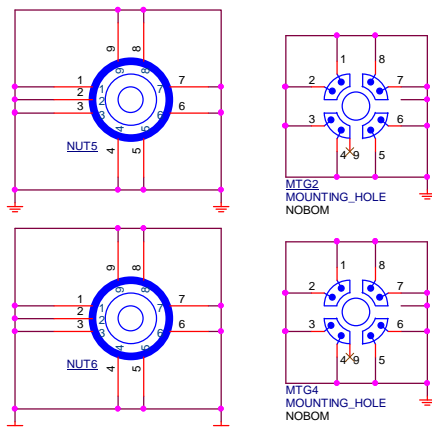
CPU COOLER



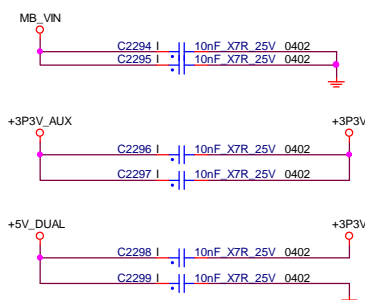
BOOT BLOCK ENABLE



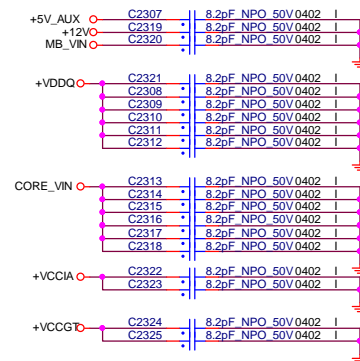
SCREW HOLES



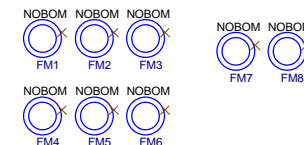
Stitching Cap



RF Add Cap



OPTICAL POINT




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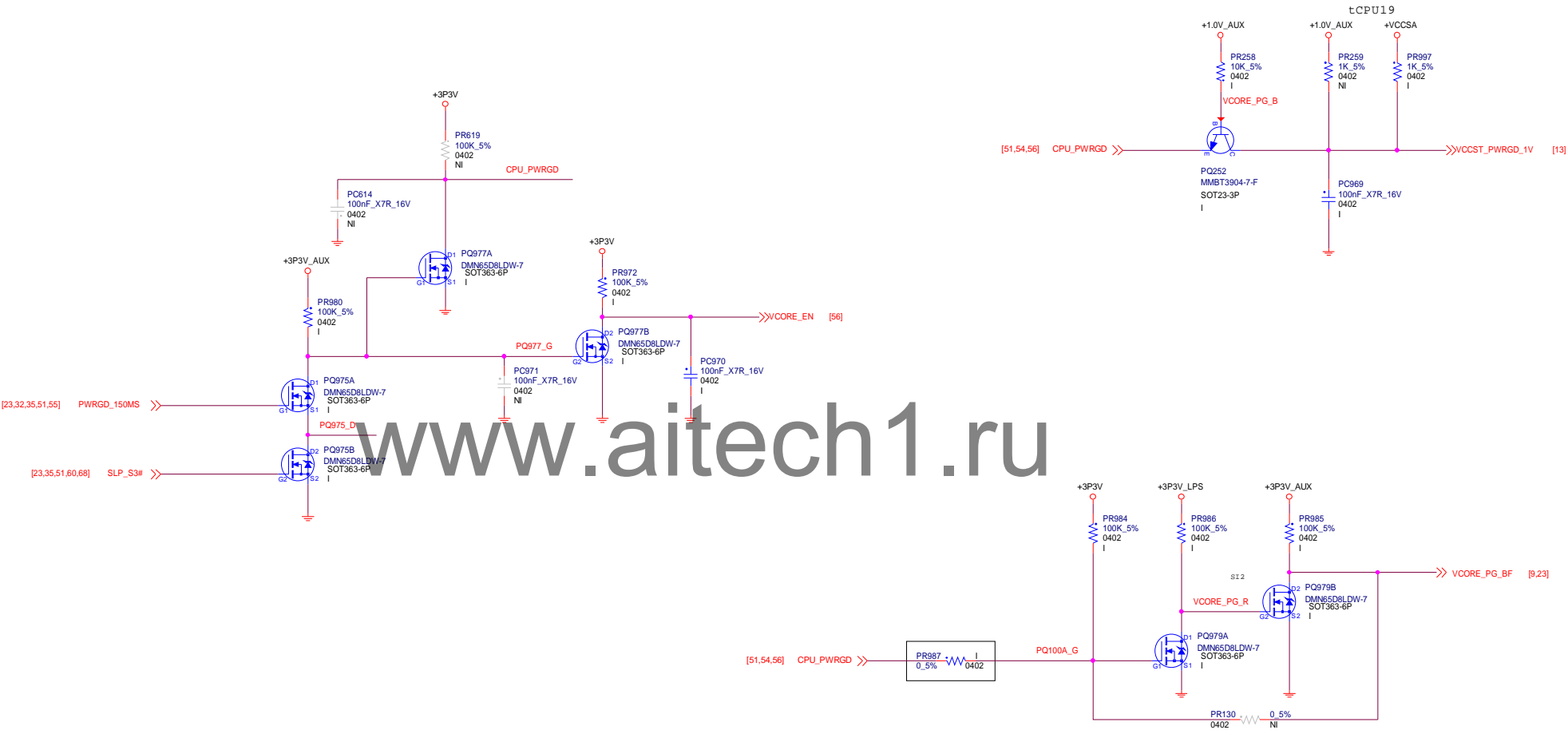
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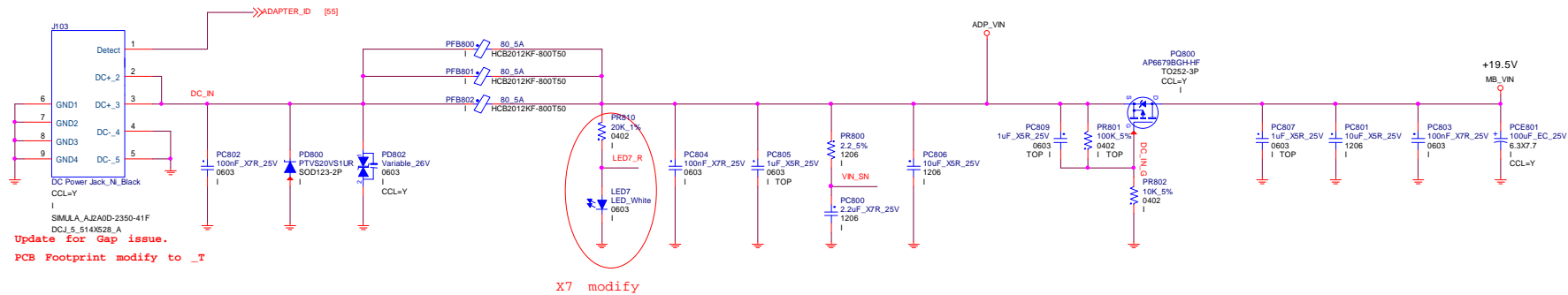
Place the circuit here for VCORE sequence reference.



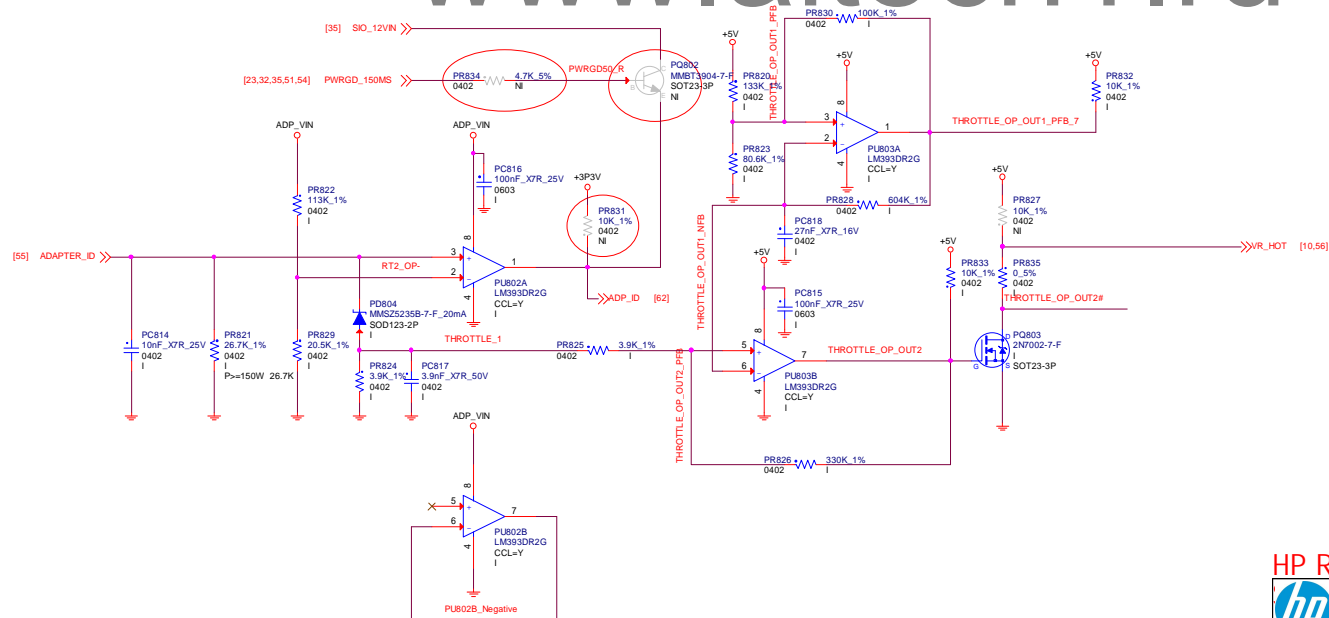
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| Title POWER SEQUENCE | | | |
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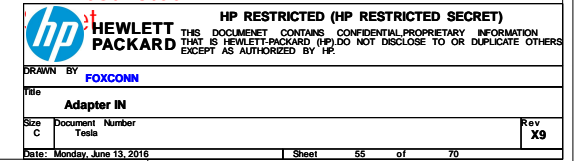
19V DC Power Adapter-in



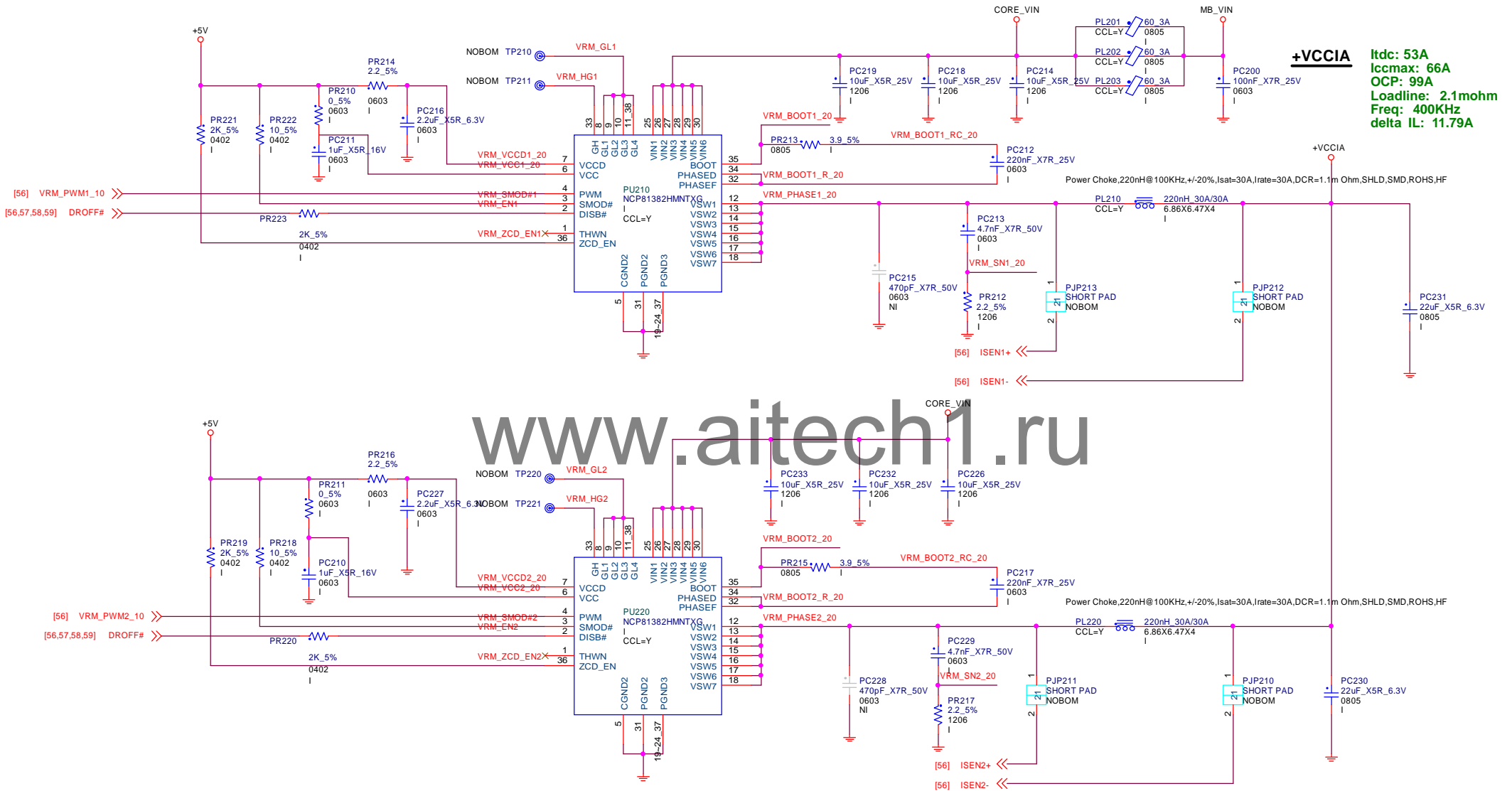
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VCORE PHASE1~2



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VCORE PHASE3



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+VCORE PHASE 3

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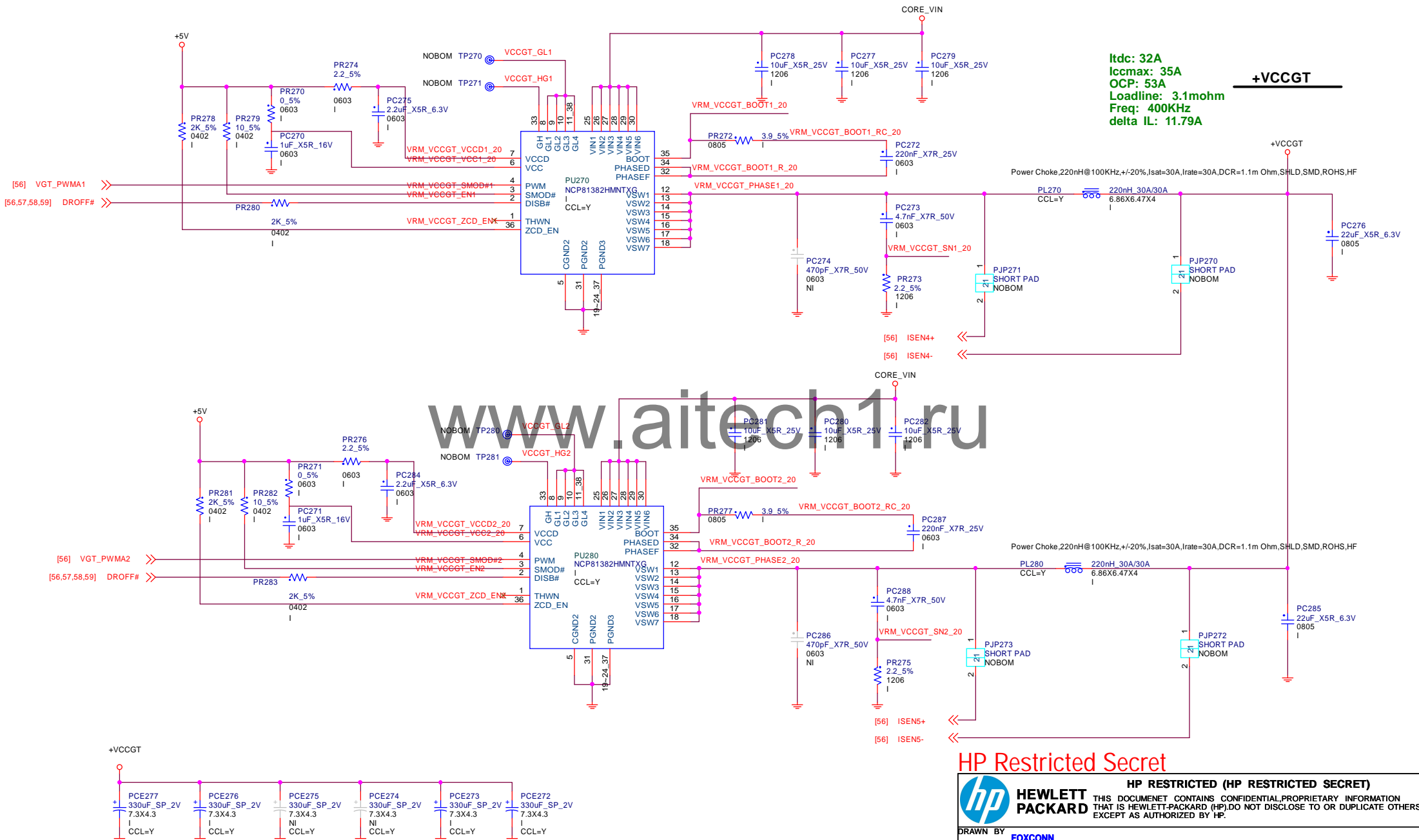
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|-------|----|----|----|

X9


VCCGT PHASE1~2

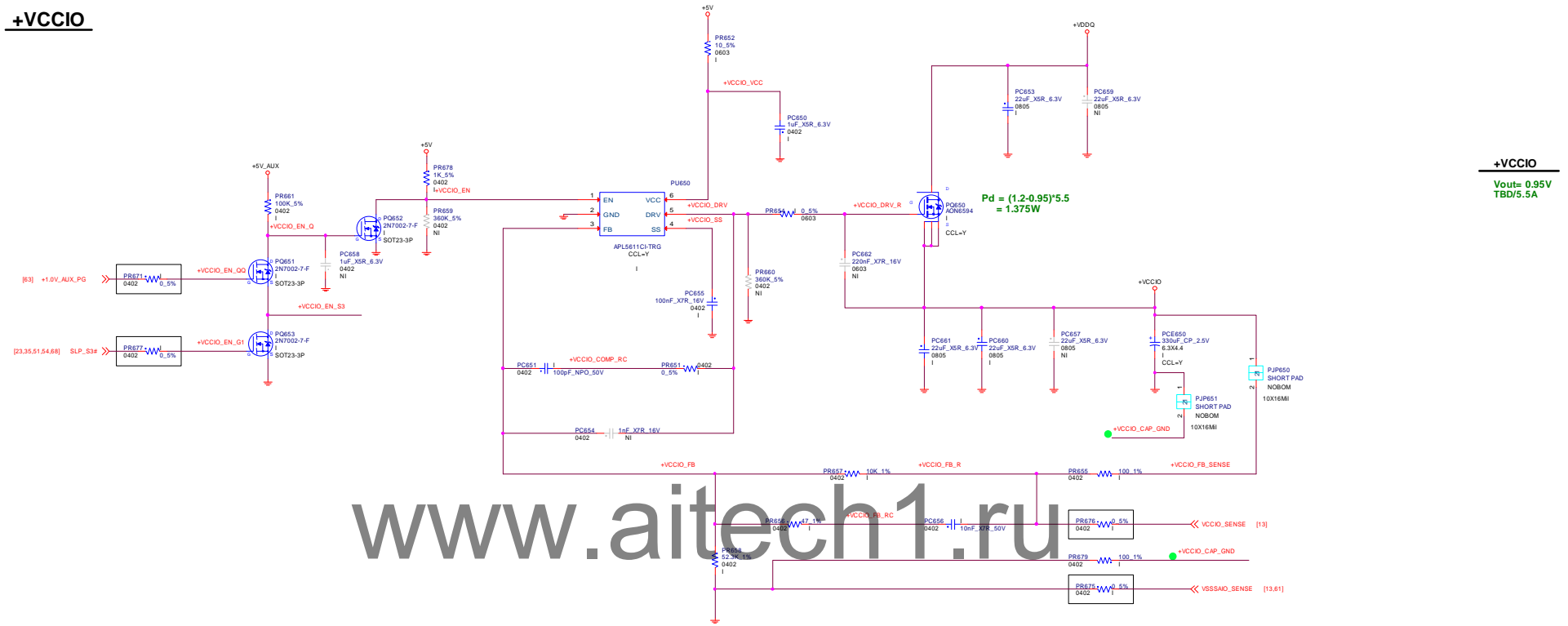


It'dc: 32A
Iccmax: 35A
OCP: 53A
Loadline: 3.1mohm
Freq: 400KHz
delta IL: 11.79A


+VCCGT

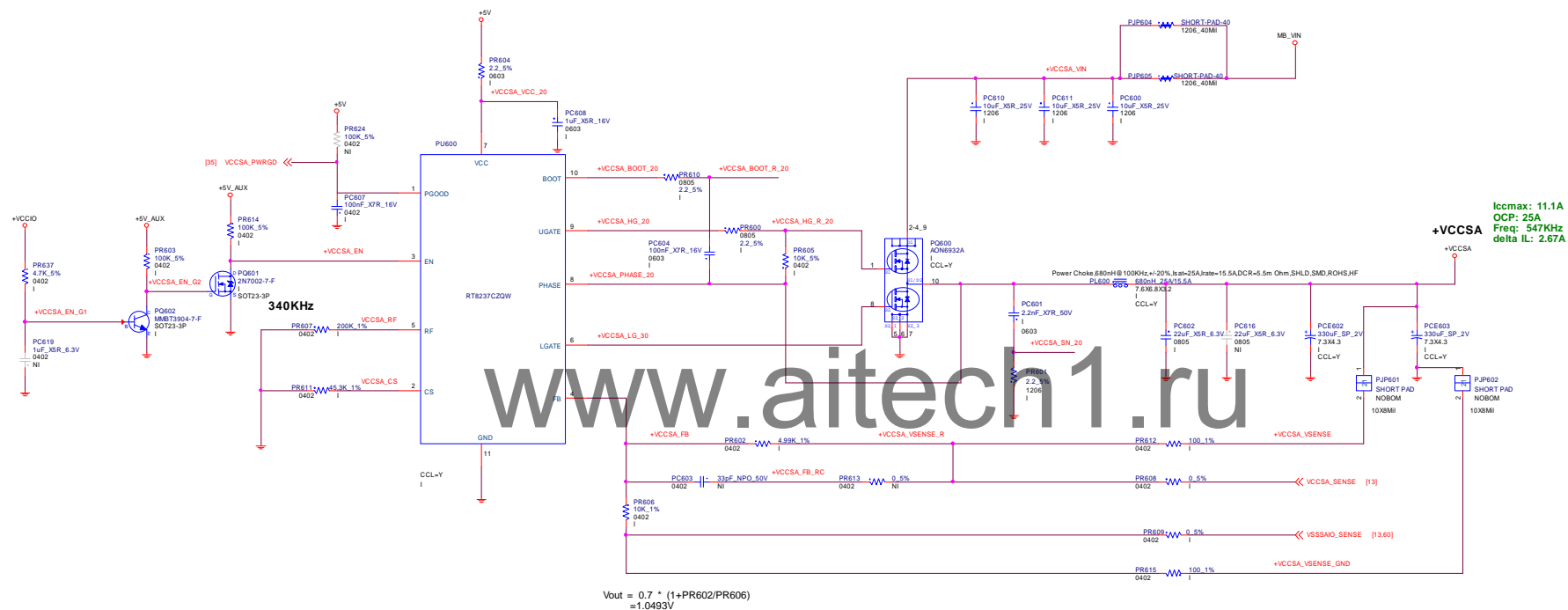
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| Title <div style="text-align: center; font-weight: bold;">+VCCGT Phase 1 & 2</div> | | |
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| Date: Monday, June 13, 2016 | | Sheet 59 of 70 |

+VCCIO

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| | | Rev X9 | |

+VCCSA
$$V_{out} = 0.7 \cdot (1 + PR602/PR606) = 1.0493V$$

lccmax: 11.1A
OCP: 25A
Freq: 547KHz
delta IL: 2.67A

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+VCCSA

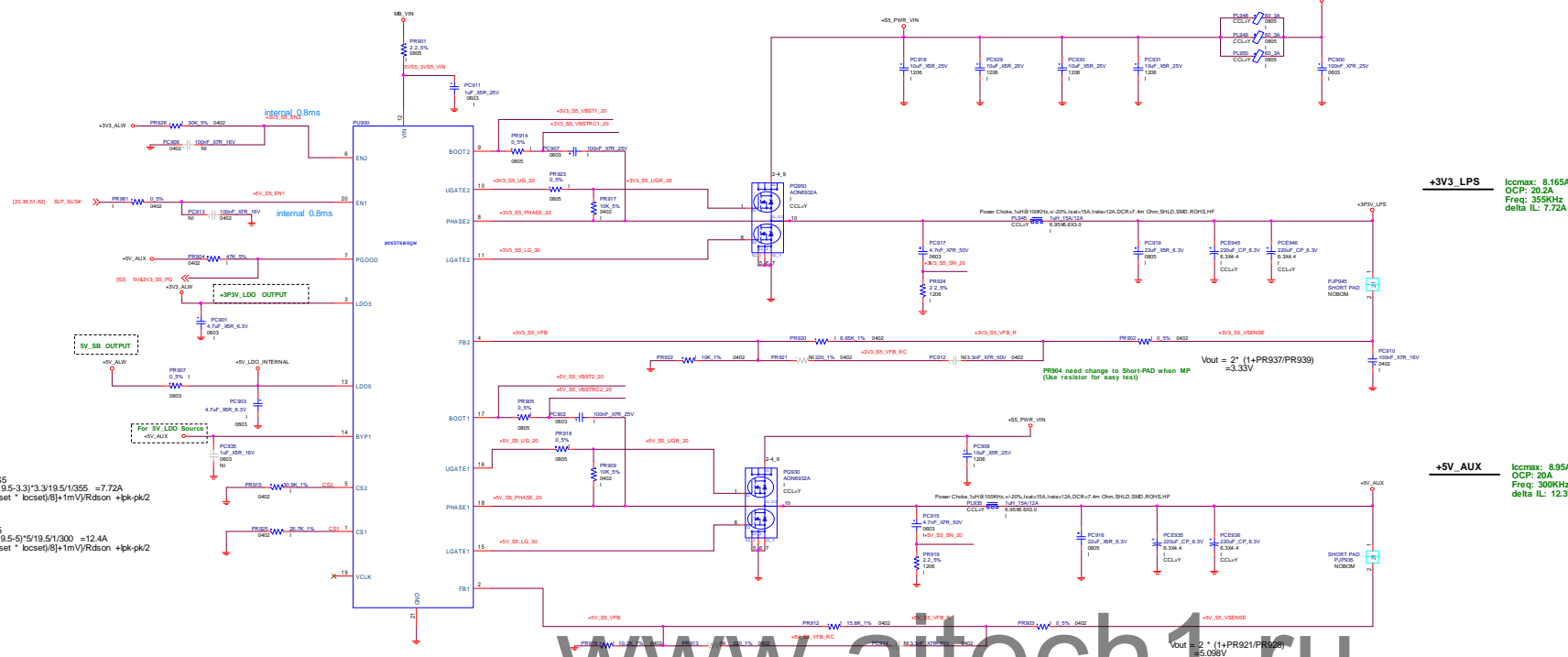
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| | |
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| | 710 |
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Note: net-name:+3P3V_A/+5V_A

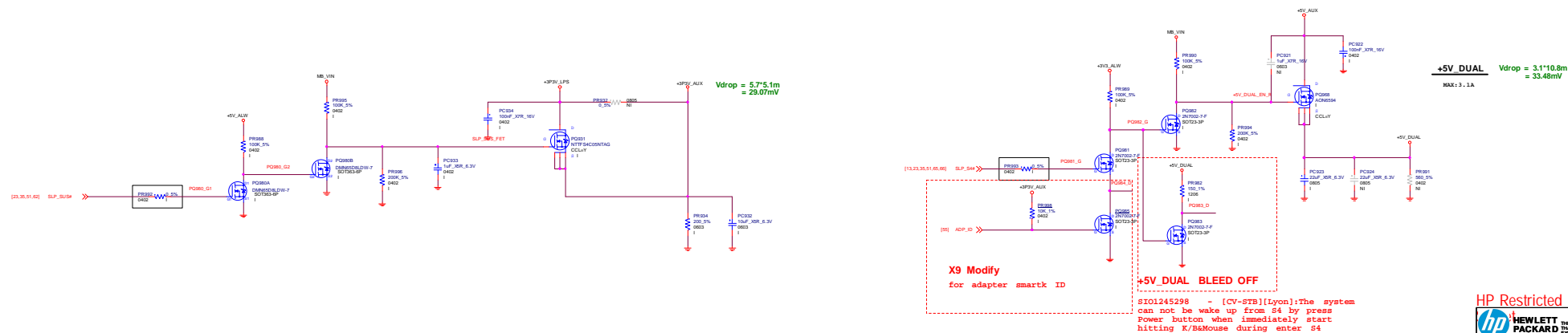


+3V3_LPS

lccmax: 8.165A
OCP: 20.2A
Freq: 355KHz
delta IL: 7.72A

+5V_AUX

locmax: 8.95A
OCP: 20A
Freq: 300KHz
delta IL: 12.3



X9 Modify

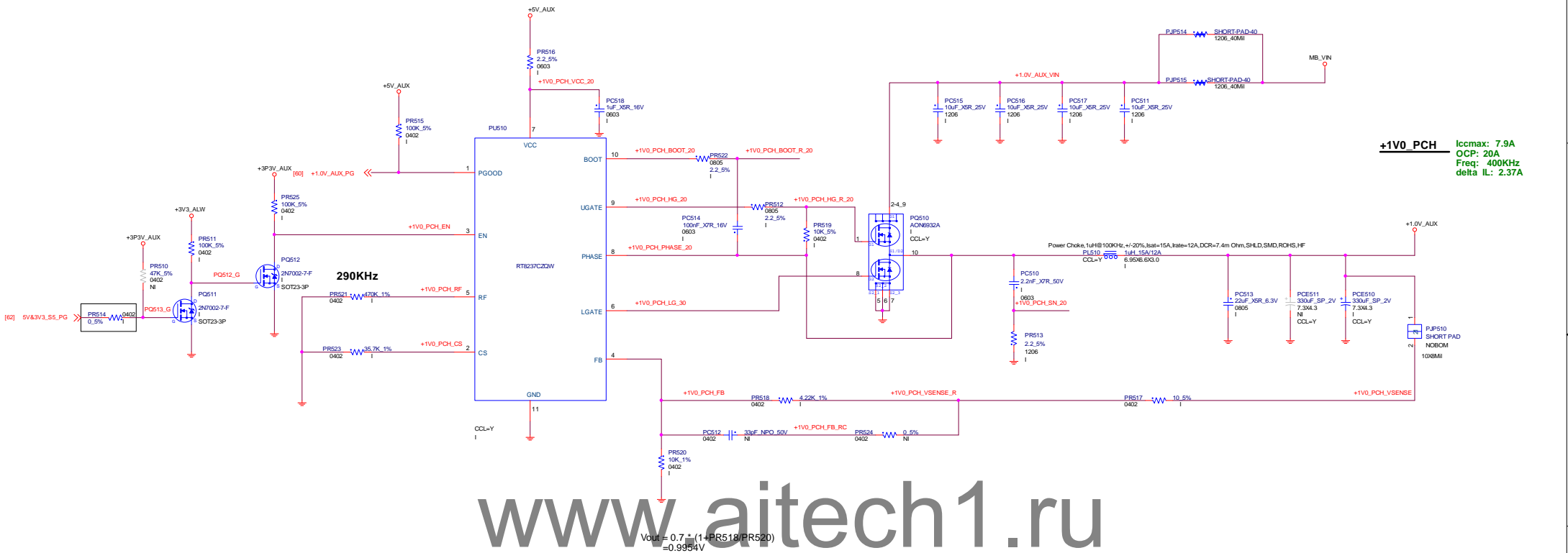
+5V_DUAL BLEED OFF

SIO1245298 - [CV-STB][Lyon]:The system can not be wake up from S4 by press Power button when immediately start hitting K/B&Mouse during enter S4

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| Title +1V_PCH | | | | | |
| Size | Document | Number | Rev | | |
| Custom | Testa | | X9 | | |
| Date: Monday, June 13, 2016 | | | Sheet | 63 | of 70 |

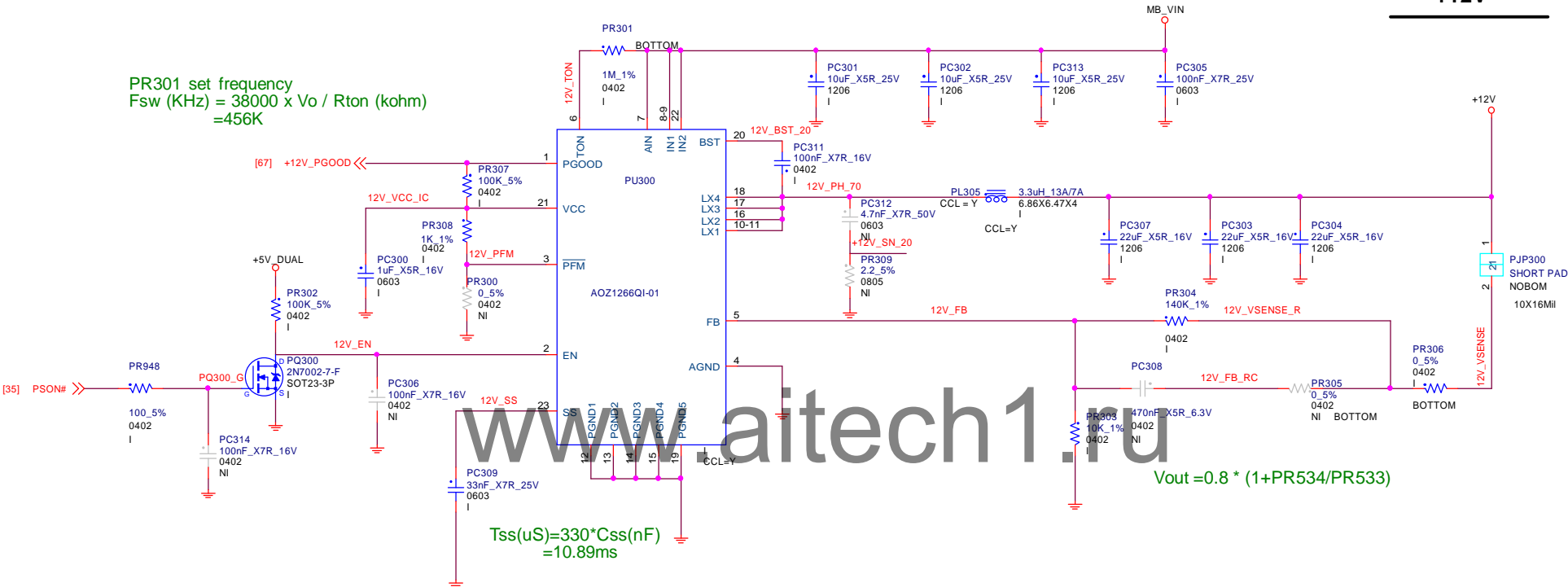
Note: net-name:+12V

PR301 set frequency

$$F_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$$

$$= 456 \text{ K}$$

Iccmax: 0.68A
 OCP: 9.5A
 Freq: 456KHz
 delta IL: 3.07A



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+12V

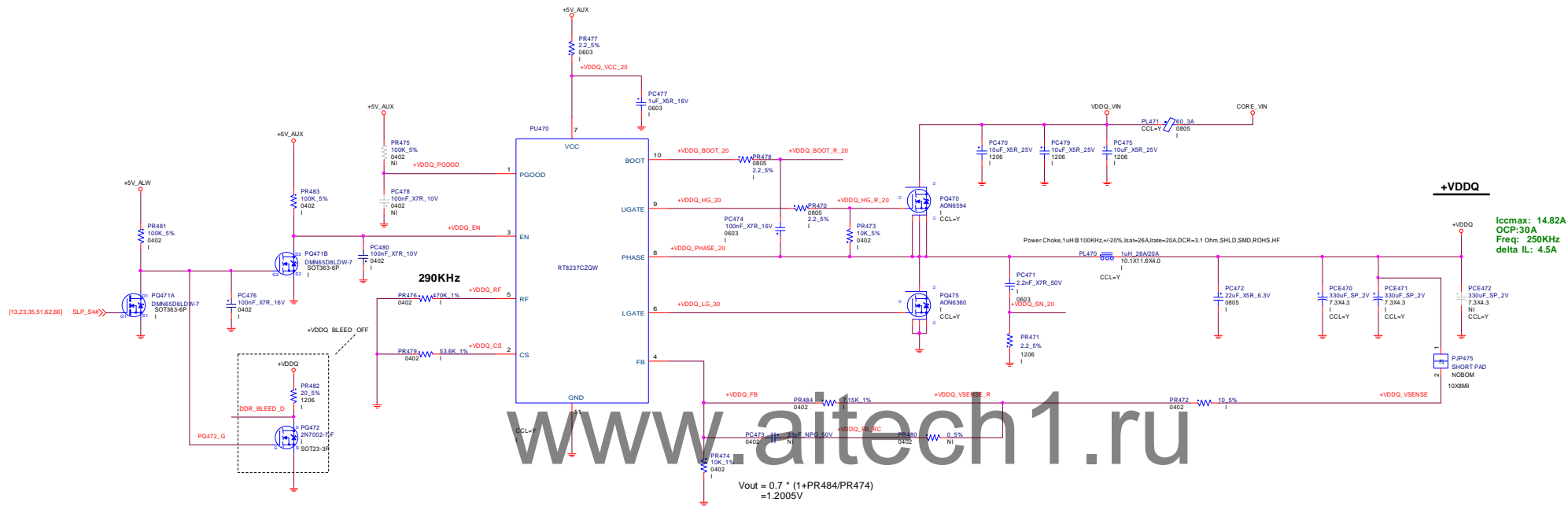
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Date: Monday, June 13, 2016

Sheet 64 of 70

Rev
X9

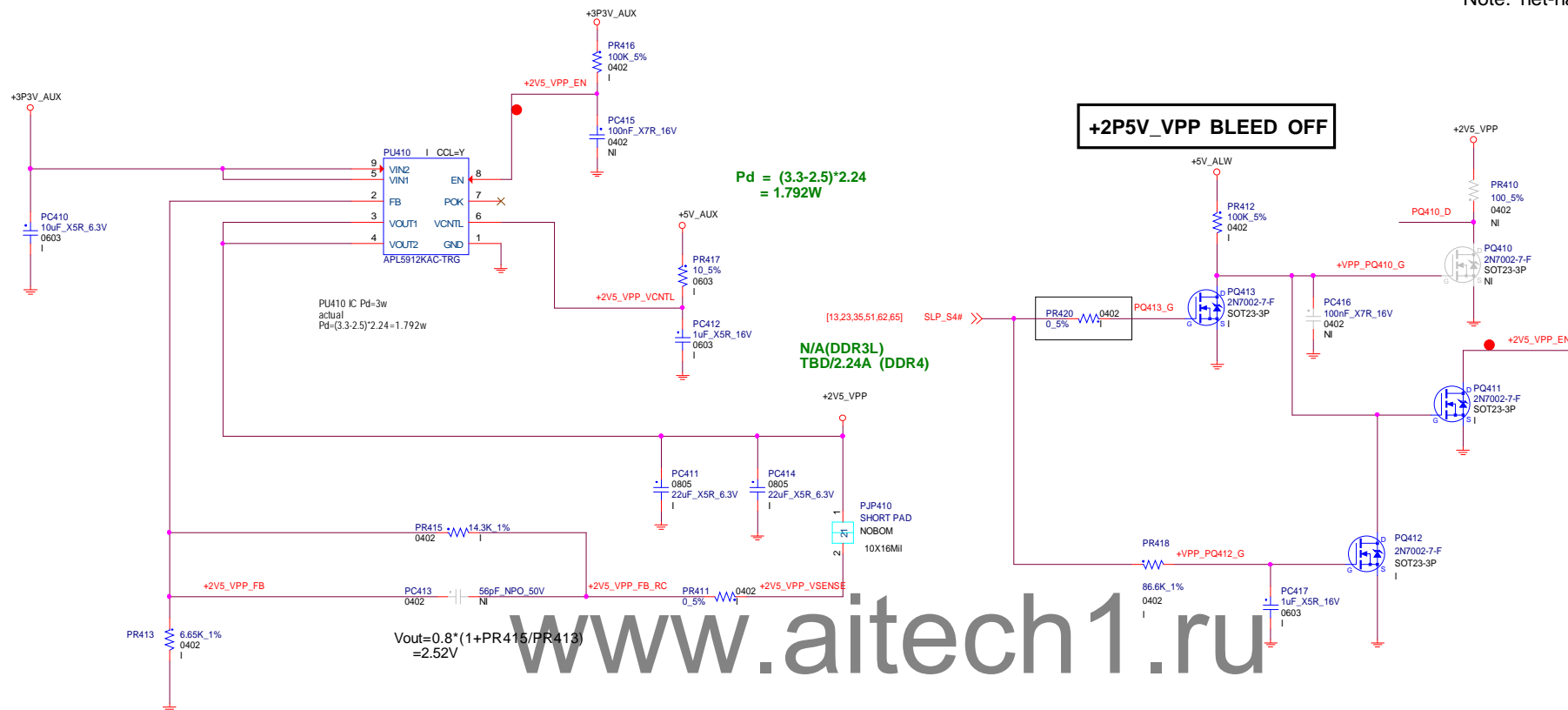
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+VDDQ

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| Custom | Tesla | | |
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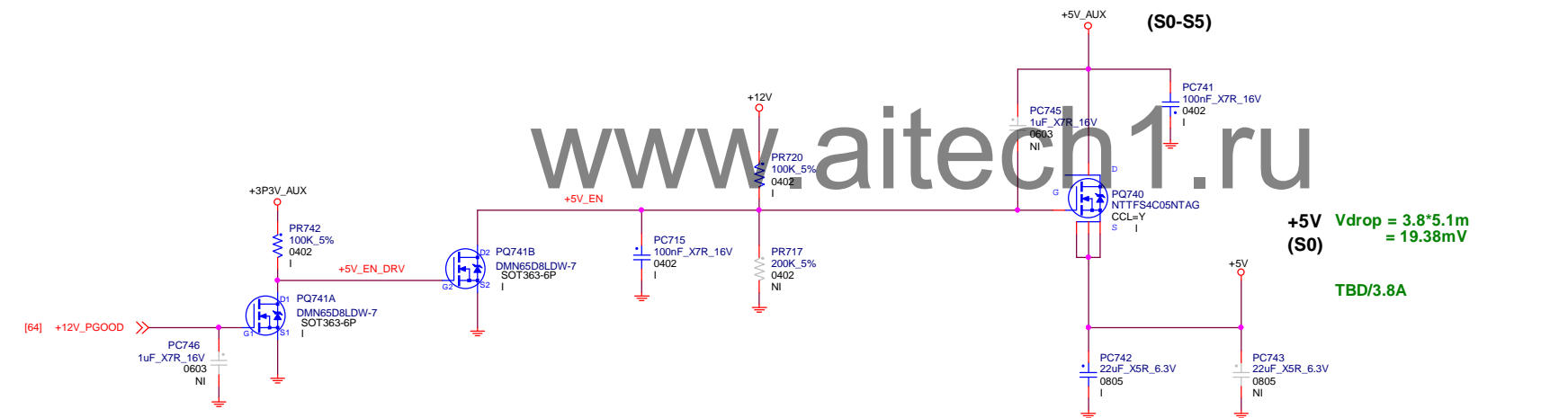
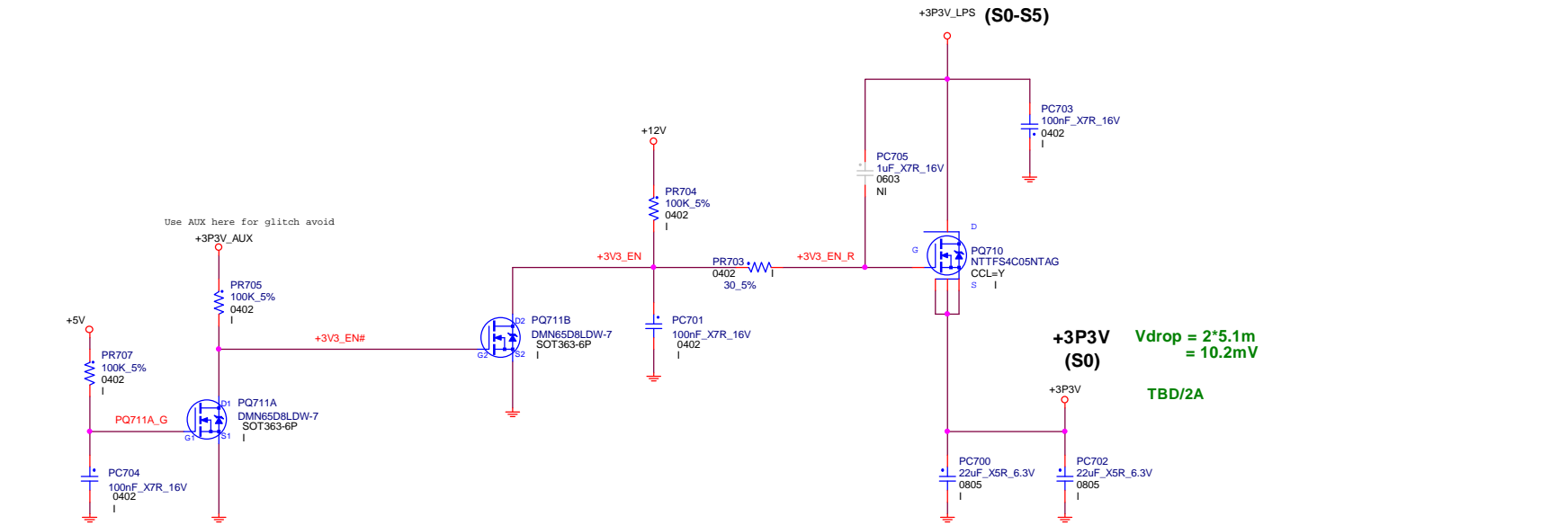
Note: net-name:+2V5_VPP




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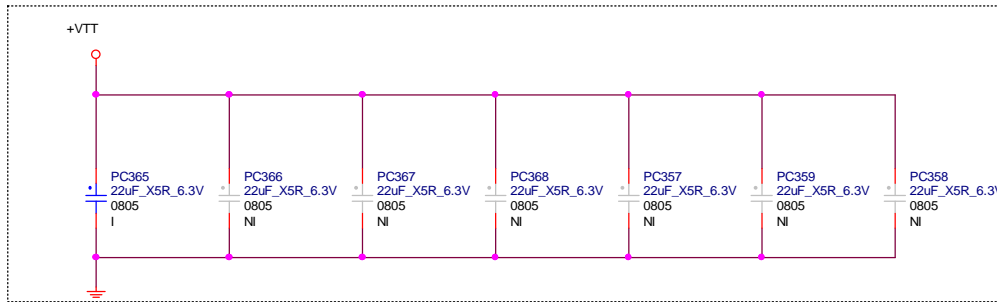
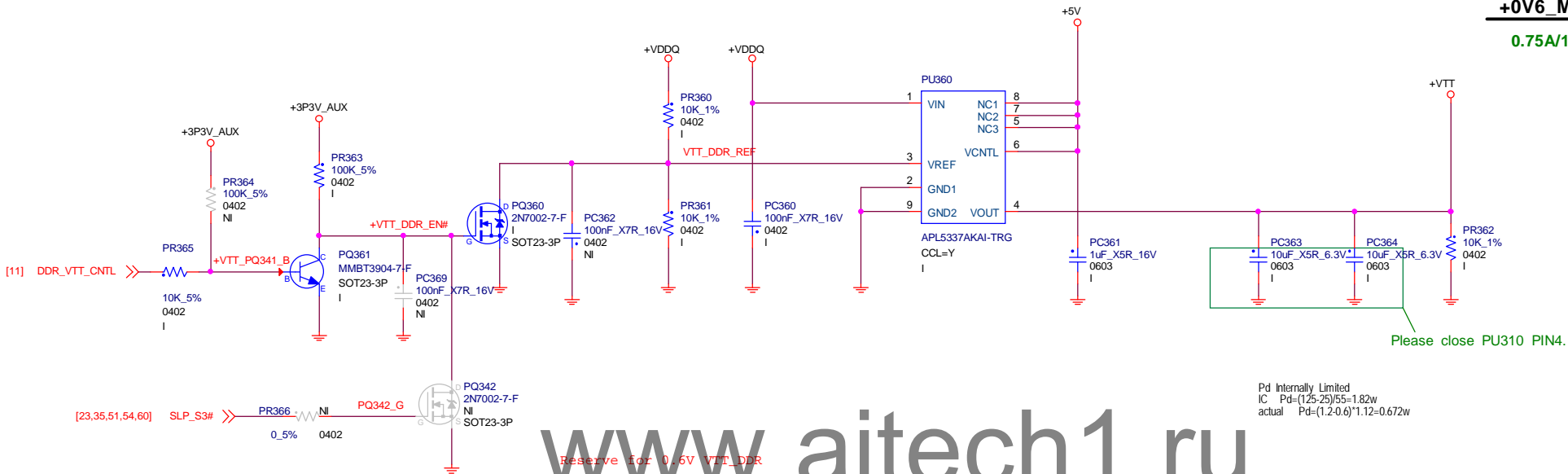
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+VTT_DDR

+0V6_MEM

0.75A/1.12A



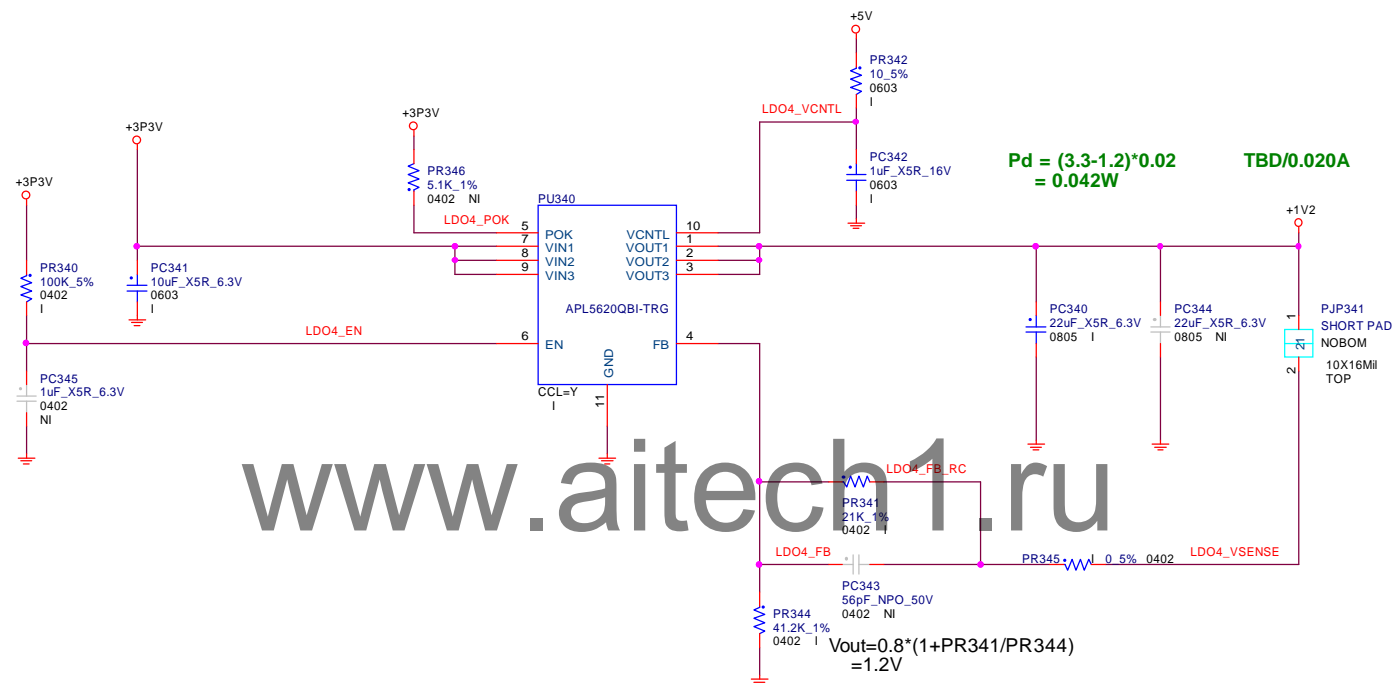
The Qty output cap should be careful
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG
1.0 for Aztec City CRB

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+1V2



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| Size | Document | Number | Rev | | |
| Custom | Testa | | X9 | | |
| Date: Monday, June 13, 2016 | | | Sheet | 69 | of 70 |

DB FAB Change list

[illegible]

X3 conn. gap Modify list

| | | | | | |
|----------|--------|--------|---------|-----|-------------------------|
| 20161229 | Monday | ASAC | 264 | 949 | |
| | | SP | 263 | 948 | |
| | | USAC | 262,293 | 940 | for test cum cap issue. |
| | | Type 0 | 2215 | 943 | |
| | | CR | 2266 | 931 | |

X4 D&D Modify list
31160134 2021/03/

| | | | | | |
|----------|--------|--------------|-----------------------|--------------------|-----------------------------|
| 20160114 | Modify | sys | PLANNING/WORKING PLAN | addition delete | 805 |
| 20160114 | Modify | GUI | GUI | addition delete | AGC3241 AGC3245 |
| 20160115 | Modify | system power | R/A | P62 | Change P9900 to HT557680QM. |

X6 21 Modify list

[illegible]

| ST | IPV | Modify | List | reference | substate | Page | Description |
|----------|-----|--------|--------|-----------|----------|------|------------------------|
| | | Date | Action | | | | |
| 20100428 | | Modify | | | | 314 | add QPS NC delay acth. |
| 2010428 | | Modify | | | | 315 | Improve QPS temp. |
| 2010428 | | Modify | | | | 313 | add de pop acth. |
| 38 | MMB | Modify | List | | | | |
| | | Date | Action | reference | substate | Page | Description |
| 20100531 | | Modify | | | | 313 | MMT update MM |

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Rev **CHANGE LIST**

| Rev | Document Number | Rev |
|-----|-----------------|-----|
| 0 | 0 | XS |
| Rev | 0 | 0 |